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Ph.D. THESIS

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Medium voltage power converters with SiC power devices

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Abstract

Title: *Medium voltage power converters with SiC power devices*

The thesis presents considerations regarding power electronic systems based on Silicon Carbide power devices dedicated to applications in the medium voltage range. More specifically, the topics under consideration are modeling of medium voltage SiC power devices, focusing on the characterization method for the transistor output capacitance, used for accurate switching loss determination; a power loss estimation method for converters, established on a simple experimental setup; a comprehensive study, founded on experimental models, for various converter solutions dedicated for medium voltage power electronics with SiC power devices, including two-level, multilevel, series connection, and quasi-two-level methods; and novel approaches for dc-dc converters converging soft-switching techniques with the quasi-two-level method, aiming at improving the efficiency and power density. The dissertation consists of five core publications, which are preceded by an introduction briefly describing the subjects, the primary motivation for the specific concepts, an overview of the prior findings from the literature, as well as accentuating the contribution of the papers. Even though SiC power devices have been researched for several years, there are still limitations to the proper utilization of Silicon Carbide power devices for medium voltage applications, such as adequate semiconductor modeling, accurate power loss estimation, or the choice of a suitable topology. Thus, these issues are addressed within the thesis. All in all, it is shown that employing SiC-based power devices provides a myriad of opportunities for medium voltage power electronics applications, such as improved efficiency or higher power density, which surpasses the formerly-used Silicon-based power electronics.

Keywords: *electric energy conversion, multilevel converters, power electronics, power converters, SiC MOSFET, series connection of power transistors.*

Streszczenie

Tytuł: *Przekształtniki energoelektroniczne średniego napięcia z przyrządami mocy z węglika krzemu*

W rozprawie przedstawiono rozważania dotyczące układów energoelektronicznych dedykowanych do pracy w zakresie średnich napięć i wykonanych z wykorzystaniem półprzewodnikowych elementów mocy z węglika krzemu. Praca zawiera opis modelowania przyrządów mocy pracujących w przekształtnikach średniego napięcia z elementami z węglika krzemu, skupiając się na metodzie charakteryzacji pojemności wyjściowej tranzystora, wykorzystywanej do dokładnego określania strat łączeniowych; metodę estymacji strat mocy w elementach przekształtnika opartej o prosty układ eksperymentalny; studium porównawcze oparte o modele eksperymentalne dla różnych rozwiązań przekształtnikowych dedykowanych dla energoelektroniki średniego napięcia z uwzględnieniem wykorzystania tranzystorów mocy obejmujących układy dwupoziomowe, wielopoziomowe, a także oparte o szeregowe łączenie i metodę quasi-dwupoziomową; oraz nowatorskie rozwiązania przekształtników prądu stałego łaczące techniki miękkiego przełączania i sterowania quasi-dwupoziomowego, mające na celu poprawę jego sprawności i gęstości mocy. Rozprawa składa się z pięciu głównych publikacji, które poprzedzone są wstępem krótko opisującym tematykę, główną motywacją przedstawianych koncepcji, przeglądem dotychczasowych dokonań z literatury naukowej, a także zaakcentowanie kluczowych osiągnięć w artykułach. Mimo że elementy półprzewodnikowe z węglika krzemu są badane już od kilku lat, to nadal istnieją istotne ograniczenia, takie jak nieprecyzyjne modelowanie półprzewodników, niedokładne określanie strat mocy, czy wybór odpowiedniej topologii przekształtnika. Tym samym, kwestie te zostały poruszone w pracy. Podsumowując, wykazano, że zastosowanie przyrządów mocy z SiC w zastosowaniach energoelektroniki średniego napięcia umożliwia m.in.: poprawę sprawności i/lub uzyskanie wyższej gęstości mocy, przewyższając parametry uzyskiwane przez układy zbudowane z elementów mocy wykonanych w technologii krzemowej.

Słowa kluczowe: *energoelektronika, przekształtniki energoelektroniczne, przetwarzanie energii elektrycznej, SiC MOSFET, szeregowe łączenie tranzystorów mocy, przekształtniki wielopoziomowe*

Abbreviations

BJT	bipolar junction transistor
DFIG	double-fed induction generator
EMI	electro-magnetic interference
ESS	energy storage system
FACTS	flexible AC transimission systems
FC	flying capacitor
GTO	gate turn-off
IGBT	insulated gate bipolar transistor
IGCT	integrated gate commutated thyristor
JFET	junction field-effect transistor
LV	low voltage
ML	multilevel
MMC	modular multilevel converter
MOSFET	metal-oxide semiconductor field-effect transistor
MV	medium voltage
NPC	neutral point-clamped
PMSG	permanent magnet synchronous generator
PWM	pulse-width modulation
RES	renewable energy sources
SC	series connection
Si	silicon
SiC	silicon carbide
SST	solid-state transformer
TCM	triangular current mode
THD	total harmonic distortion
QSW	quasi-square wave
WBG	wide band-gap

Contents

Chapter 1

Introduction

Medium voltage level has always been the most common choice for high-power power electronics applications, which is mainly associated with reduced current levels compared to low voltage systems. Smaller currents lead to significantly reduced conduction power losses, leading to better efficiencies, and also decreased volume and weight of the conductors - cables or busbars. The interest in MV power electronics has been gaining even more traction lately, as the global aims for decarbonization of society and the industry are becoming more important every year. To reduce the CO_2 emission levels, the one target is the successful implementation of renewable energy sources, such as wind, solar, and hydropower plants, as the core generation sources since conventional energy sources, such as coal plants, are a source of extensive pollution, and do not correspond to the environment-friendly policies, such as Fit For 55, currently considered in the European Union. Taking into account the two most common RES - the wind and solar systems, the former has been mostly bound to MV levels since its inception, and the latter has also recently been introduced into a higher voltage range with PV strings rated at 1.5 kV and above. Moreover, the trend of reaching for higher and higher voltages every year is a recurring theme also for other systems, e.g., battery energy storages.

However, renewable energy sources are not the only applications for MV power electronic converters. A large variety of other applications employ such a voltage range. To name a few, e-mobility and electrical traction can be considered, as well as high-power motor drives, data centers, or smart grids. Considering the vast amount of power processed through these applications, energy conservation via more efficient means of energy conversion is also a focus to reduce the emission levels.

Therefore, there is a great need for efficient and reliable MV power electronics, preferably with limited volume and little effect on the surroundings, e.g., through electromagnetic or acoustic interference. The conventional approach to constructing medium voltage power

electronic converters is to use power semiconductor devices based on well-known Silicon technology, usually in the form of IGBTs, GTOs, or IGCTs. However, the advances in WBG semiconductor technology, and especially Silicon Carbide, have brought the well-performing MOSFET into the medium voltage range. While currently available devices are bound to up to 3.3 kV breakdown voltage, the prototypes of devices rated at 10 kV and above have already been presented. Even though higher voltages can already be reached with Si devices, SiC brings many other advantages compared to standard Si-based semiconductors. Namely, they are characterized by better switching capabilities, lower power losses, as well as higher sustainable temperatures, which provide the possibility to construct MV power converters with substantial power density and extremely high efficiencies. SiC-based power devices have already surpassed state-of-the-art Si-based counterparts in many ways, and it is predicted that they will even become more auspicious in the future.

While plenty of MV SiC-based power converters have already been presented both in academia and industry, there are still many issues to be resolved before the entirely appropriate employment of SiC semiconductors in MV power converters can be achieved. For example, since the rapid switching of SiC devices induces much more severe issues with parasitic components in the circuits, special care has to be given to the hardware design of the system. Moreover, the more complex structure of the SiC chips requires the introduction of new models and characterization methods. Furthermore, this can also be analyzed from a more general perspective: What topologies and control methods would result in the most efficient converters when SiC power devices are employed? Of course, this is just the tip of the iceberg, and the possible research opportunities seem nearly endless.

Thus, there is still a need to investigate SiC-based MV power electronic systems further so that full utilization of WBG power semiconductors can be achieved and sought-for, highly-efficient and compact MV power converters can be constructed.

The thesis outline is as follows. After a brief introduction showcasing the importance of MV power converters in today's society, a more thorough overview of power electronic applications is presented. It starts with the presentation of a plethora of MV systems that employ power converters. Then, the significance of the emerging Silicon Carbide semiconductor technology in MV is shown, especially considering the possible advancements over conventional Silicon-based power devices and the SiC-specific issues that are still to be resolved to utilize the technology fully. Further, the possible approaches to construct power converters employing SiC power devices are analyzed, focusing on different topologies. At last, the first part of the dissertation is finalized with the motivation behind the thesis and its aims.

In the second part of the dissertation, the contribution of the author within specific subtopics on MV SiC-based power converters is presented based on publications included in the thesis. The first area of interest is the modeling of medium voltage SiC power devices and converters, including the power loss estimation, where two papers are shown and briefly described. Further, the topic of topology concepts for MV power converters is considered and shown based on a publication considering several different approaches. In the next part, an exemplary MV dc-dc converter is exhibited, employing a novel topology and control scheme, utilizing the many advantages of SiC power semiconductor devices. This area is supported by two papers.

In the end, the thesis is concluded, showcasing that employing SiC-based power semiconductor devices helps to construct highly-performant MV power electronic systems, especially in terms of efficiency and power density, that easily surpass their Si counterparts.

1.1 Power electronic applications in medium voltage range

Global energy consumption is rising every year, with a rate of roughly 4% increase annually [1]. As can be seen in Fig. 1.1, a significant part of the share at 45% is due to industrial and transportation uses, which often employ MV systems.

At the same time, environmental concerns necessitate serious alterations in the global energy system, for example, through the shift of the energy sources from fossil fuel-based systems to RES or in the form of preserving the energy through more efficient conversion. While the current RES share in the global energy production is just slightly above 10%,

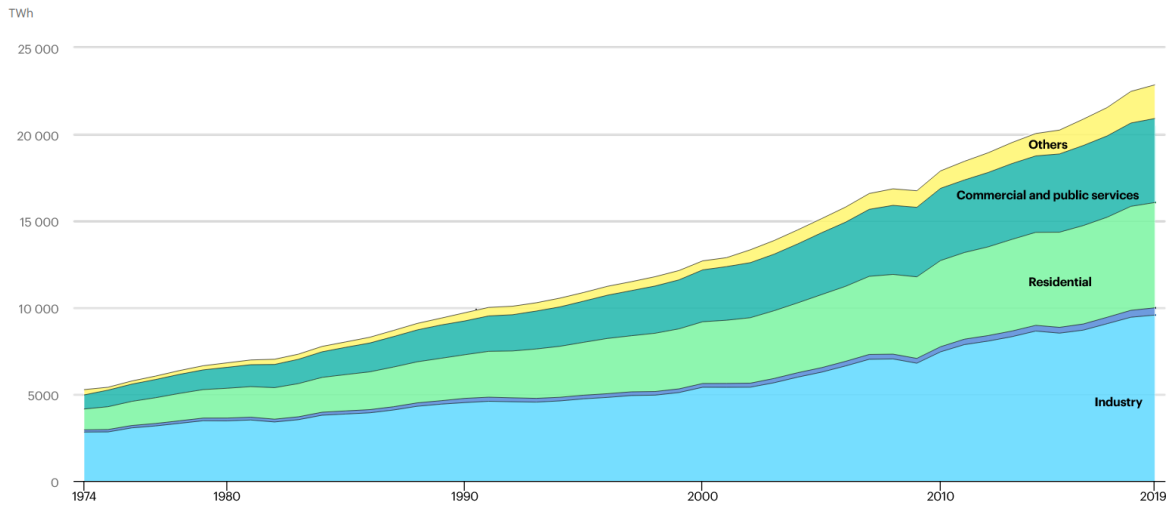

Figure 1.1: World electricity consumption by sector, 1974-2019 [1].

"global renewable capacity is expected to increase by almost 2 400 GW (almost 75%) between 2022 and 2027 in the IEA main-case forecast" (Fig. 1.2) [2]. Thus, the constantly increasing worldwide interest in RES requires more sophisticated power conversion systems, as well as a more decentralized approach to power systems, which also need to consist of distribution means based on power electronics, such as smart grids that usually favor MV instead of HV.

Furthermore, nowadays, almost every newly installed power system facilitates some kind of power electronics, either to increase their performance or to enable higher flexibility. Hence, there is a vast area for MV power converter applications, ranging from industry applications through e-mobility and transportation, RES, distribution and generation, and many, many more (see Fig. 1.3); which are addressed in the following in more detail.

Starting off, RES systems are considered an emerging topology for MV power electron-

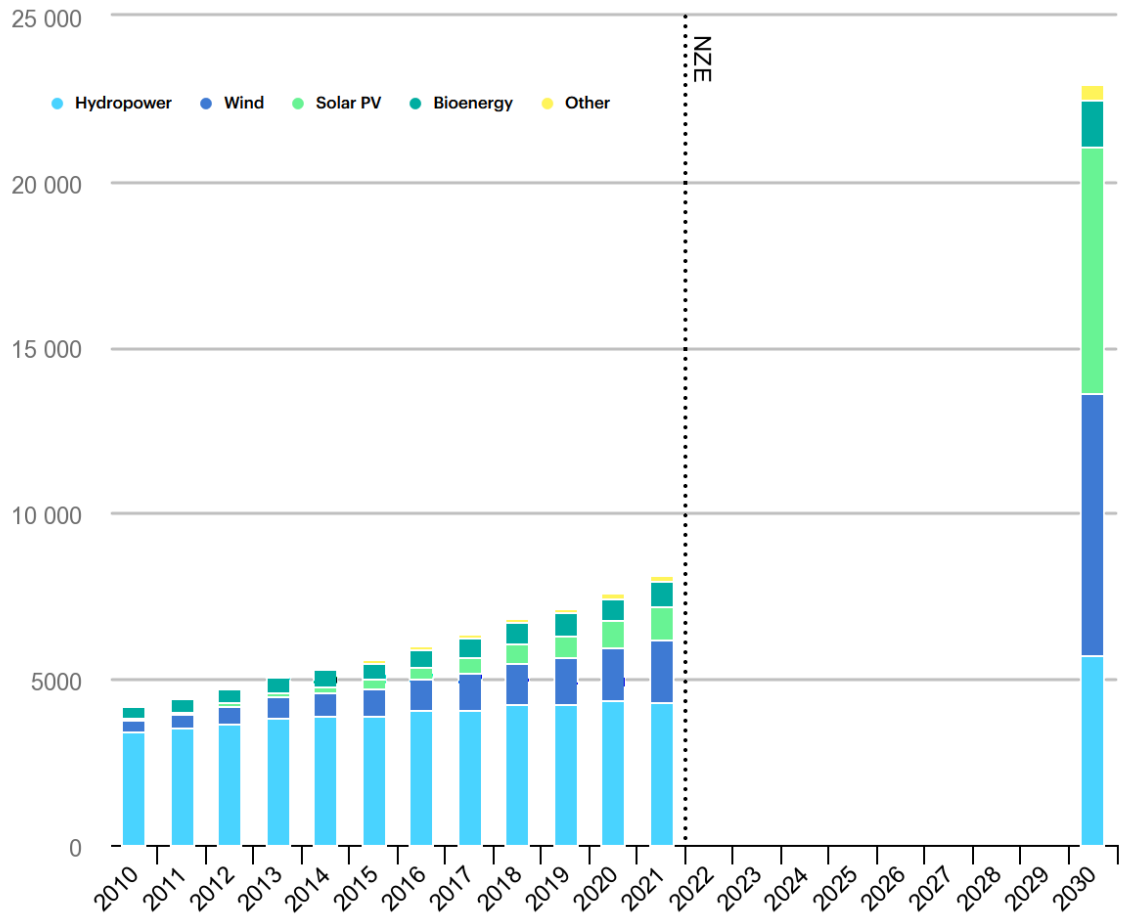

Figure 1.2: Renewable power generation by technology in the Net Zero Scenario, 2010-2030 [2].

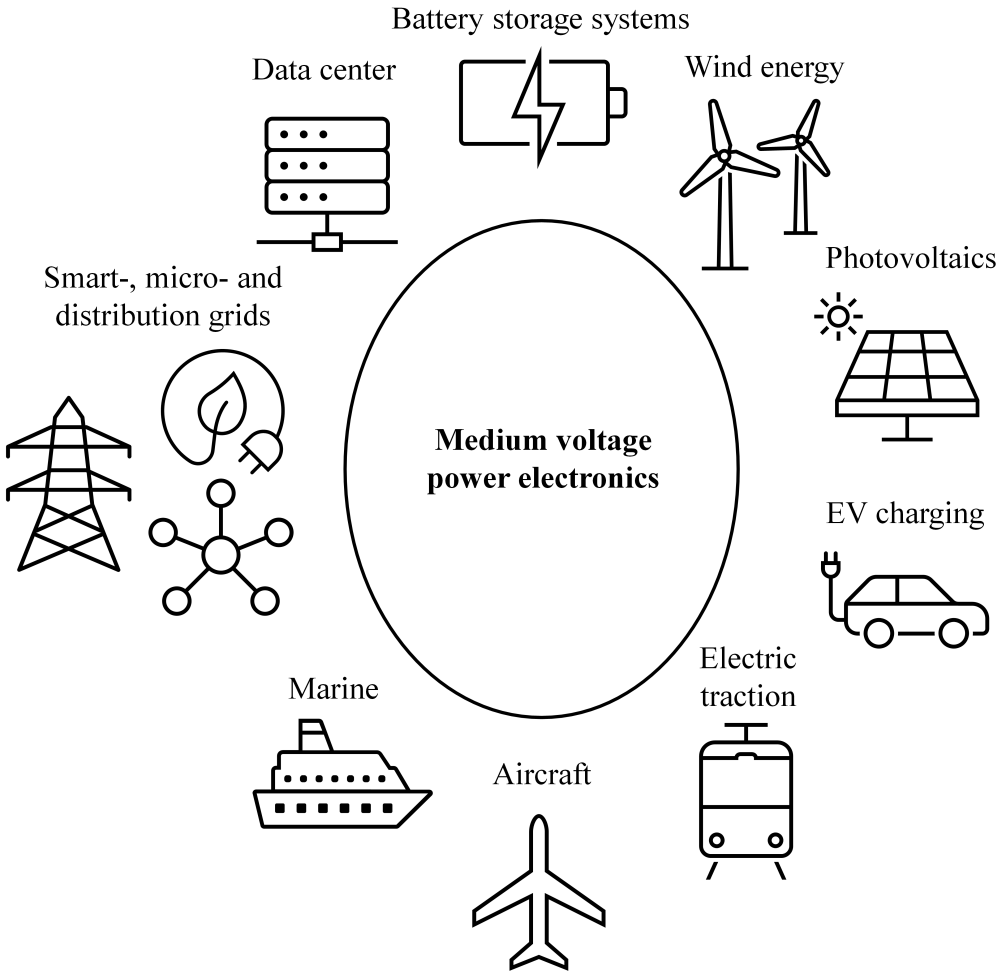

Figure 1.3: A vast application range for MV power electronics.

ics. Wind energy harvesting employs MV levels for the wind turbines almost exclusively because of the expedited power levels, ranging from several hundred kW up to single MW [3]. Nowadays, the most common solution is a full-scale converter paired with either DFIG or PMSG so that a frequency decoupling between the motor and the grid is ensured, along with an extra opportunity for THD improvement. The dominant converter topologies currently include multilevel approaches, usually in ac-dc-ac configuration [4].

Recently, PV systems are also under consideration for MV expansion. Taking into account substantial PV power plants, MV collector grids are often considered for multi-string connection and grid integration [5, 6]. In this case, large-power SST systems are of interest, aiming at efficiency and mains current quality. On the other hand, MV is also introduced into single PV strings, with voltages as high as 1.5 kV already established [7]. However, for this kind of application, dc-dc non-isolated converters capable of managing the high PV voltage fluctuation are being considered.

With the introduction of more and more RES into the electric power systems of the future, which can be quite unpredictable in regard to providing a reliable power supply, and moving further away from conventional, stable fossil-based power plants, the mismatch between the power demand and availability may become higher every year. Already today, there are often fluctuations ranging from too much generation (e.g., from PV systems that have to be shut down to not exceed the grid voltage) to insufficient power that could potentially lead to blackouts. Therefore, MV ESS has to be included in power systems of the future [8], while these are also already considered for other applications, for example traction grid support [9, 10] or to supply the energy for heavy-duty electric vehicles [11]. In general, ESS can be categorized into two groups: those that require high power capability in a short span of time, e.g., employing battery stacks or supercapacitors for either load leveling or peak shaving applications, and the less frequent solution of long-term energy storage by means of, for example, pumped-storage hydroelectric systems. Depending on the type of the ESS and the grid connection, both dc-dc and ac-dc systems are considered.

With the rapid increase of EVs on the global market, a requirement for fast and reliable charging stations arises. In order to have EVs fully replace conventional internal combustion engine-based vehicles, there is a need for ultra-fast charging stations, which are capable of charging the batteries to 90% of SOC in about 10-15 minutes [12]. To achieve such results, a power of several hundreds of kW per vehicle is required. Thus, since the whole charging station power range resides in MW, a direct connection to the MV grid is a common choice [13]. Therefore, grid MV converters are a necessity, often also with bidirectional capability supporting vehicle-to-grid operation or in an SST topology. Moreover, MV level is also considered for the DC distribution grids for EV charging stations [14], with the mentioned requirements for MV dc-dc converters as well.

Supplying the power to the rolling stock is also a domain of MV. The traction grid voltage levels and type can vary; 1.5 and 3 kV DC lines are used in certain countries such as Poland, Italy, or France, while AC systems with 15 and 25 kV are commonly used in Switzerland or Germany. Furthermore, MV is also sometimes adopted for metro or tram lines, e.g., metro lines in China with 1.5 kV DC. Therefore, both ac-dc and dc-dc power converters are employed as the front-end for supplying the power. Furthermore, considering that trains use several types of power electronic applications, such as power drives, auxiliary converters, and ESS, a wide variety of power converters are required.

Amidst the e-mobility applications, aircraft seems to be far from all-electric implementation. This is sourced in the serious concern for the weight and volume of the system, which is currently highly limited because of heavy batteries, power electronics, as well as electric

machines [15]. However, there are concepts for all-electric aircraft, and these use MVdc grids as a core with voltages as high as 10 kV [16, 17], requiring formidable support from dc-dc and dc-ac power converters. Nevertheless, either in current, jet engine-based, or future, all-electric aircraft applications, the use of MV power inverters for electric drives is a necessity.

Similarly, as in the aircraft applications, marine power electronics are also bound to MV voltage levels due to very high power ratings of megawatts and higher. Again, MVdc grids for energy distribution are considered, with voltage reaching 20 kV [18]. MV power inverters are also employed for variable frequency drives used in marine vessels [19]. All in all, even though the base characteristics and converter types are akin to the aircraft applications, because of the weight constraints, the end-product power electronics systems will vary vastly and require an individual approach.

Besides transportation uses, such as in the aforementioned aircraft and marine applications, MV motor drives are also vastly employed throughout the industry, with different power, torque, and speed requirements. To name a few, the mining, metal, oil, and gas industries can be distinguished, as well as water and chemical applications [20]. Therefore, there is a great emphasis on the MV power converters for electric drives.

Currently, over 1% of global energy is used in data centers [21]. This number is growing every year, especially with rapidly growing computational requirements, e.g., due to the employment of artificial-intelligence-driven applications throughout many aspects of our lives, starting from research, through industry, and up to personal use for entertainment. Even though at an end-level, these type of applications uses thousands of LV small-scale converters, the foundation of the system is a front-end grid converter, usually interfacing an MVac grid with voltages of around 10-20 kV, with an LVdc grid at the level of 400-800V [22]. Thus, MV SST ac-dc converters are of great interest.

The emerging technology concepts in the form of smart grids, fulfilling the roles of distribution and collector grids, interfacing RES and ESS, and many more, also favor MV levels due to increased flexibility compared to HV grids [23, 24]. Furthermore, constant progress in power electronics and semiconductor devices helps accentuate the advantages of MV over HV. An MVdc system can be employed as an interfacing grid between the HV transmission system and the many applications from its surroundings, e.g., RES, ESS, active compensation systems, as well as industry and residential loads [25]. The shift from an ac grid to a dc system leads to a more straightforward integration of generation and load systems, employing power converters without frequency synchronization and/or reactive power compensation. Furthermore, a lower number of conversion levels can also be achieved, leading

to increased efficiency. However, the installation cost of such a smart grid is high compared to a conventional approach.

As mentioned previously, MVdc grid applications have a wider variety of uses, for both on-shore, e.g., dedicated PV or wind DC grids, and off-shore applications, such as sub-sea power distribution systems. These types of smart grids require many power electronic converters for proper operation, grid converters from basic rectifiers to inverters; dc-dc converters, non-isolated and isolated, bi- and unidirectional; more sophisticated SST, and various protection and auxiliary systems.

Historically, DC grids were limited in voltage, which can be observed using the traction grid as an example, where the highest common voltages for AC and DC-type traction are 25 kV and 3 kV, respectively. The most visible bottleneck causing the limit in voltage for DC systems is the fact that natural zero crossing of the fault current in DC grids does not occur. This has drastically limited the interest in MVdc systems as conventional circuit breakers employed in ac systems are based on that phenomenon. However, with the advances in CB concepts, WBG semiconductor technology, fault detection in MVdc systems is becoming possible [26]. Therefore, as also mentioned before, MVdc grids are gaining more traction throughout many applications.

In order to sustain constantly increasing influence of distributed generation, as well as to counteract the negative influence of applications with noisy current draw, active compensation of harmonics of the grid currents is required [27]. In contrast to large-scale FACTS systems employed in HV transmission and distribution grids, lower-scale MV systems will have to be employed in MV grids. These applications support the grid, for example, by increasing the voltage quality through reactive power compensation or harmonic distortion minimization. These systems can take form in various ways, e.g., series, shunt, back-to-back, or multi-terminal configurations [28]. However, each system is still based on some kind of a power electronic system rated at MV.

Thus, as discussed, there is a plethora of MV power electronics applications for nearly every conversion type: isolated and non-isolated, bidirectional, and unidirectional; ac-ac, ac-dc, dc-ac, and dc-dc, with various and often distant requirements and characteristics. However, employing SiC-based power semiconductor devices instead of conventional Silicon counterparts may be deemed beneficial for each and one of them.

1.2 Silicon Carbide power devices advancing medium voltage power electronics

Inevitably, considering the vast application range of power electronics at medium voltage level, the requirements for the power converters, and specifically power semiconductor devices, can also vary intensively from application to application. However, the most common requirements for power switches employed in medium voltage converters can still be easily named and are depicted below:

- High breakdown voltage,
- Fast switching – low switching energy
- Low conduction power losses,
- High-temperature capability,
- High reliability,
- Low cost.

Even though a specific set of preferred characteristics cannot be defined in general, one trait is vital for each application in the medium voltage range – high voltage blocking capability. Even with power semiconductor devices able to block several kilovolts, building two-level converters for the whole voltage range is impossible – converter topologies employing several power switches are needed. Thus, the higher the breakdown voltage, the lower the number of devices in a stack and the lower the system's complexity. Therefore, this characteristic is beneficial for all types of converters, from conventional topologies to advanced MMC systems.

Considering MOSFETs, the high current capability is not a precisely defined parameter of the device but rather is decided considering power loss and dissipation characteristics. Furthermore, parallel connection is generally seen as easy to implement in this case. Thus, to reach higher currents, simply the chip area of the power device is increased. Hence, the power losses are an important factor for the power devices. These are generally split into conduction losses associated with on-state voltage drop and switching losses depending on the turn-on and turn-off switching energy and the operating frequency. While minimizing power losses is an aim for most systems, the choice of a specific device varies depending on the application characteristics. For example, inherently soft-switching converters usually favor devices with minimized conduction losses, while the switching loss is not essential, as

these are vastly minimized anyway. Similarly, circuit breaker applications are not concerned about the switching loss since switching is not apparent during most of the operation.

Another trait strictly connected with the losses is the switching speed of a device. From one point of view, a higher switching speed results in a smaller overlap of voltage and current and leads to lowered power losses. Furthermore, shorter switching time allows for higher operating frequencies, which may lead to smaller passive components and enhanced system power density. On the other hand, higher switching speed may lead to issues with EMI, as the parasitic components become more crucial. Thus, this aspect also depends mainly on the type of application.

While the size of the chip is relatively small compared to other components of medium voltage power converters, it can still be important performance-wise, especially considering the aforementioned impact of parasitics. Moreover, the device's volume is often also directly connected with the power dissipation capabilities and the connections, which is especially vital for power modules that contain several chips within its structure, often employed in the medium voltage range. Overall, a small footprint and size of the device may be an important factor for certain applications.

Several medium voltage applications need to operate within harsh environments, e.g., in underground conditions, as in mining, or some automotive applications. In such cases, the temperature capability of the power devices can be a defining factor.

All the applications ideally should operate as reliably as possible. However, for some systems, it is more important than others. While a failure of part of a data center or one charger in a big EV station is not preferable, it does not lead to a crisis. On the other hand, a breakdown of an electric drive in a factory causes notable financial repercussions, while a malfunction of the electric system in an aircraft may even lead to catastrophic results with the cost of human lives.

Eventually, financial concerns are obviously an important aspect as well. Again, while in general, the lower the cost, the better, some applications may favor price over every other trait, while a different one would not consider price as a crucial factor.

All in all, each power device requirement can be considered more or less important for each system. Therefore, the choice of a specific power device for a defined application should be performed in accordance with its benefits and deficiencies. As an example, high-power applications favor the use of thyristors, as these are characterized by high voltage blocking levels and current capabilities. On the other hand, MOSFETs have relatively low voltage blocking proficiency, but they exhibit superior switching performance, while IGBTs are a middle ground between these two options. Finally, the introduction of the WBG power

semiconductor technology, specifically SiC for medium voltage converters, allows for the construction of devices with higher blocking voltage capabilities and introduces the aforementioned MOSFETs into medium voltage range.

When most of the aforementioned requirements are concerned, the emerging silicon carbide technology seems to be a superior option compared to conventional silicon-based power devices - see Fig. 1.4. While Si technology has been well-established since the inception of power electronics in the 1960s, it simply cannot compete with SiC-based devices when medium voltage is considered, as the performance of the WBG counterparts is far ahead of the state-of-the-art Si power semiconductor devices in almost every aspect [29, 30], such as lower power losses, higher operating frequencies, and better temperature capabilities, while lagging behind primarily because of the relative immaturity of the technology – thus the cost is much higher, and the reliability is still a concern. However, as the technology improves, the drawbacks become less severe year-by-year [31], and thus SiC is the power device of choice for power electronics today, and even more so in the future [32, 33, 34, 31, 35] – see Fig. 1.4.

The story of power devices in Silicon Carbide technology begins in the 1990s when first analyses and concepts were shown [36], exhibiting the material's potential. However, it took many years from the concept level to actual device prototypes, and the first SiC devices were available on the market in the 2000s, namely SiC diodes and JFETs as the transistors [32]. However, because of the normally-on behavior of the JFETs, these have been quickly surpassed by MOSFETs, which have become the most popular SiC device to date, as they exhibit similar, exquisite performance but with normally-off operation. There have also been SiC BJTs presented; however, since voltage-controlled transistors are preferred, these have also quickly been pushed out by the MOSFET. Finally, the still-dominant technology in Silicon – the IGBT – has yet to be fully introduced onto the market with Silicon Carbide. While

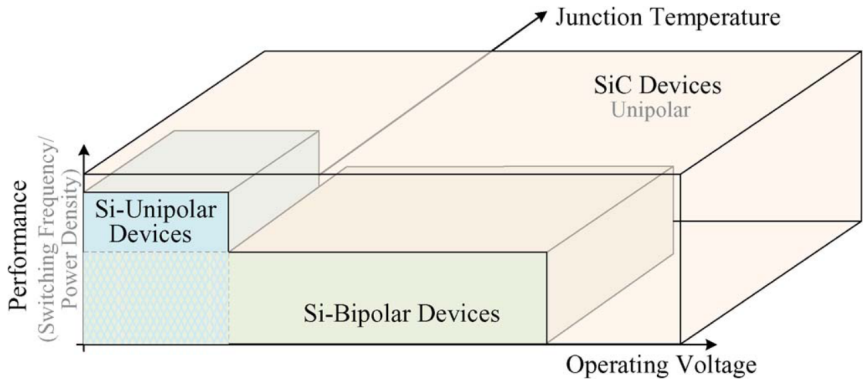

Figure 1.4: The potential of Silicon Carbide technology over Silicon [29].

there have been prototypes reaching as high as 27 kV breakdown voltage [37], the manufacturing process is still far from commercialization, e.g., because of the intrinsic defects in the chips [38].

Focusing on the most popular type of power device, the SiC MOSFET, currently, there are commercially available transistors reaching as high as 3.3 kV [39], with prototypes at even 15 kV [40], that slowly begin to push out its Si-based counterparts. However, there is still room to improve as there are well-known, reliable, and proven Si devices in the form of Si IGBTs and Si thyristors. On the other hand, considering devices at 1.2 kV breakdown voltage and lower, SiC devices have already become the device of choice for LV power electronics and can be widely found not only in academia but also in industry applications [33].

That is due to the vast advantages of the SiC-based devices compared to their state-of-the-art Si adversaries, as has been proven by many works [29, 41, 30]. The many advantages include, amongst many, higher sustainable voltages, higher possible switching frequencies due to faster switching speeds and lower switching losses, minimized conduction losses as an effect of material properties, and higher tolerable junction temperatures. These provide the possibility to increase the converter performance, efficiency, as well as power density. The performance ratings are even more advantageous for the SiC over Si when MV is considered, as there are only bipolar devices available for the Silicon technology, and these are naturally less capable compared to unipolar devices.

The outstanding characteristics of SiC-based devices are inherently connected with the superior material properties of the WBG technology. More specifically, Silicon Carbide is distinguished by a larger (wider) band-gap, higher critical field, greater saturation velocity, and better thermal conductivity [36, 35].

The practical differences between power devices, both in Si and SiC technology, can be easily observed when comparing commercially available components rated at similar power level, both for discrete devices, as well as power modules. Table 1.1 depicts the parameters of two state-of-the-art 1.2 kV-rated discrete transistors in TO-247-4 packaging from the same manufacturer (on-semi) – FGH4L40T120LQD (Si IGBT) [42] and NTH4L040N120M3S (SiC MOSFET) [43]. As can be seen, considering the performance parameters, the SiC-based device is superior. The on-state losses are lower (16 vs. 25 W), the switching losses are almost ten times smaller, and the switching time is much shorter, with 72 ns compared with 339 ns of the Si IGBT. Furthermore, the gate charge is also much decreased, allowing for easier driving of the transistors. On the other hand, when the cost is considered, SI IGBT is cheaper. However, since 1200 V-class transistors in SiC are already well established on

Table 1.1: Si IGBT and SiC MOSFET power device comparison for discrete transistors rated at 1.2 kV in TO-247-4 package, provided by the same manufacturer. [42, 43]

Device type	Discrete transistor	
Package	TO-247-4	
Manufacturer	on-semi	
Device no.	FGH4L40T120LQD	NTH4L040N120M3S
Type	Si IGBT	SiC MOSFET
Breakdown voltage	1200 V	
On-state resistance (MOSFET) at 20 A	-	40 $m\Omega$
Saturation voltage (IGBT) at 20 A	1.25 V	-
Estimated on-state loss at 25 °C, 20 A	25 W	16 W
Total switching time at 25 °C, 600 V, 20 A	339 ns	72 ns
Switching losses at 25 °C, 600 V, 20 A	1400 μJ	155 μJ
Total gate charge	227 nC	75 nC
Current price [44, 45]	8 $	24 $

the market, they are only three times more expensive for the considered case.

Furthermore, a comparison between power modules rated at 3.3 kV is depicted in Table 1.2. Again, when the performance of the device is considered, the SiC option is the obvious choice, with lower conduction losses (770 vs. 1013 W) and lower switching losses (0.63 vs. 1.36 J). However, the price disparity is even higher for power modules, as 3.3 kV SiC MOSFET power modules cost roghly ten times more than its 1.2 kV equivalents. All in all, considering both discrete devices and power modules, strictly focusing on performance, SiC devices are preferable over their Si counterparts and allow creating power converters with higher efficiencies and higher operating frequencies.

On the other hand, Silicon Carbide devices are still susceptible to certain drawbacks, mainly associated with the immaturity of the technology and its application in power electronics applications: in terms of manufacturing process of the chips and power devices [48, 49]; packaging of the devices, both in discrete and module setups [50, 51]; modeling, measurement and characterization [52, 53, 54]; as well as the design considerations for applying the SiC semiconductors into power converters to fully utilize their capabilities [55, 56].

While SiC technology has already been introduced many years ago, it is still not fully mature, especially compared to the Si devices, which have been investigated for over half a century. Thus, plenty of issues related to the manufacturing process of the SiC wafers remain. Several problems can be named: device reliability and device degradation are still

Table 1.2: Si IGBT and SiC MOSFET power device comparison for power modules rated at 3.3 kV, provided by the same manufacturer. [46, 47]

Device type	Power module	
Package	nHPD2	
Manufacturer	Hitachi	
Device no.	MBM450FS33F	MSM600GS33ALT
Type	Si IGBT	SiC MOSFET
Breakdown voltage	3300 V	
On-state resistance (MOSFET) at 450 A	-	3.8 $m\Omega$
Saturation voltage (IGBT) at 450 A	2.25 V	-
Estimated on-state loss at 25 °C, 450 A	1013 W	770 W
Rise time at 25 °C, 1800 V, 450 A	120 ns	400 ns
Fall time at 25 °C, 1800 V, 450 A	1300 ns	250 ns
Switching losses at 25 °C, 1800 V, 450 A	1.36 J	0.63 J

to be entirely determined in long-term operation [49, 57, 58], there are concerns regarding the gate oxide integrity [59, 60], near-interface traps [61], or threshold voltage instability [48]. Finally, the manufacturing process is imperfect; many production samples do not meet the specified parameters, for example, due to crystalline stacking faults, scratches, stains, or extra surface particles. Thus, the cost of SiC wafers is still very high [62]. Nevertheless, this is mostly a subject for material engineers working on power devices on a different level – thus, it is not further elaborated on within the thesis.

Packaging the power devices is also an important aspect of state-of-the-art SiC transistors, especially crucial for high-power MV power modules. Still, many current SiC devices directly adopt the packaging used for Si parts, e.g., to allow direct replacement of SiC instead of Si. However, since SiC power devices are characterized by different operating parameters, namely higher switching speeds, the parasitics of the devices and their packaging, including bonding, are the source of several issues [50, 51, 63, 64]. These include excess ringing, leading to increased EMI and additional power losses, limiting the possibilities of Silicon Carbide. This issue is specifically harmful when power modules are considered since these employ several chips paralleled to reach high sustainable currents and are usually bigger. Therefore, the path lengths, e.g., through bonding wires, are longer and induce more parasitics. Thus, there are works with improved power modules designed specifically for SiC, e.g., by employing busbar connections within the modules [65], and the subject is also considered in industry, as several companies, such as Microchip or Wolfspeed, offer SiC power modules with dedicated packaging. Still, since the packaging is also a concern for power

device manufacturers, it is not studied further in the thesis.

Considering the aforementioned traits of Silicon Carbide, as well as the structure of the chips themselves, there are plenty of concerns in regard to the proper modeling of the devices, their characterization, and methods to extract the design properties of SiC transistors to be employed in power electronics systems, namely, to precisely estimate power losses and temperatures. This is further associated with the complications regarding the measurements, for example, of the rapidly-changing currents [66].

In order to investigate power electronic systems, as well as to design highly efficient and compact power converters, simulations are the tool of choice for many engineers and researchers. Thus, power device simulation models are developed. However, considering the high-speed switching behavior of SiC-based transistors, it is not a simple task [67]. Furthermore, the models developed for Si devices cannot be applied to SiC because of the different characteristics [68]. To emulate the switching process properly, the MOSFET capacitances must be considered and modeled [54, 69]. Still, the foundation of the models is the characterization based on the measurements of the actual devices, either done by the manufacturers and provided in the datasheets or performed further by the designers, e.g., via double-pulse tests. There are several methods presented, both for dynamic [53, 70, 71], and static [72] characterization of SiC MOSFETs. However, a simple methodology for characterizing the capacitance is still lacking, as the methods are either proposed only for low-voltage discrete devices, require supplementary active circuitry, or induce the need for precise calibration of the setup. Thus, this subject needs to be further investigated.

Following the modeling, another important aspect of the design of highly-performing MV power converters is the precise estimation of power losses. In general, three main methods for determining the converter power losses can be identified: electrical-based measurements, e.g., with a power analyzer; calorimetric approach, either with full chambers or via thermal flow measurement; as well as calculations [52, 73]. While the calorimetric approach provides the losses with the lowest error [74, 75], it is a complex approach that is more feasible for already-built converters. Considering the other method, the calculations heavily rely on the models and the experimental data, which, as mentioned, is not easily obtainable [76]. Finally, electrical-based measurements are generally less accurate compared to the calorimetric approach, e.g., because of the issues with probes [77]. However, these are usually very straightforward. Therefore, there are concepts for hybrid power loss estimation methods based on converging simple hardware experiments with calculations, which could be an invaluable tool for designing MV power converters. To this end, a novel concept for such a method is further exhibited in the thesis.

As was mentioned before, the exceptional switching speeds of SiC transistors raise a challenge for the design of power converters, from the gate drivers to the power circuit, in regard to diminishing the influence of the parasitics, so that the power losses [78] and generated EMI [79] are minimized [55, 56, 80]. One branch of research in this area is focused on the gate drivers; there are methods to employ active circuits that effectively lower the undesired effects [81, 82, 83]. However, these are often very complicated in practice, and the cost for medium voltage applications with tens of power devices is very high. The most obvious approach is the minimization of the parasitics within the power circuit [84, 85, 86]. However, this is not an easy task as the considerations for each converter will be different, depending on the topology, power circuit switching loops, and others. Thus, an important question regarding the design of MV power converters remains: What power switch concepts and topologies to choose in order to fully utilize SiC-based power devices in the medium voltage range?

1.3 Power converter topologies in medium voltage

The most straightforward approach to constructing power converters is employing conventional two-level structures, often used in LV power electronics but also in a lower spectrum of MV applications [40, 87, 88, 89]. A worthy merit of this solution is its simplicity – a single power module can be used for the basic converter leg. Hence, the power circuit is minimized, limiting the influence of parasitics, and the cooling of the system can be less complex. On the other hand, properly driving SiC MOSFETs rated at tens of kilovolts is challenging, e.g., because of high dv/dt ratios [81, 90, 91]. Moreover, the cost of high-voltage SiC power modules is still immense.

Furthermore, when the MV range is taken into account, such an option is not a possibility for the higher voltages as the blocking voltage requirement exceeds the capabilities for off-the-shelf power transistors. As was already mentioned, there are SiC power devices reaching even 27 kV breakdown voltage. However, these are still being developed and are not widely available, and thus, the practical voltage limit for a single switch is much lower. Having a look at the power semiconductor device market, the breakdown voltage reaches about 10 kV for Si thyristors, 6.5 kV for Si IGBTs, and SiC MOSFETs are rated at maximally 3.3 kV. Therefore, when MV applications for voltages at 10 kV and higher, no power devices can single-handily block the required voltage. Thus, seeking other, more sophisticated power converter topologies is not only an option but a necessity for the MV range.

Hence, a number of methods to create power converters capable of sustaining higher volt-

age levels have been presented – see Fig. 1.5, where the most notable ones are considered, apart from the basic two-level topology (1.5b): conventional multilevel topologies (FCC shown here) 1.5b; series connection of power devices 1.5c; sophisticated MMC structures 1.5d; and quasi-two-level method – applicable for FCC and MMC topologies.

The first, most straightforward method for creating an MV power converter is the series connection (SC) of power transistors (Fig, 1.5c). Stacking single components in order to share the voltage stress across the elements is a well-established approach, easily incorporated for passive elements as well as non-controlled semiconductor devices, i.e., diodes. It can also be applied to active components, the power transistors. Except for the main advantage – limiting the voltage requirement of individual devices – a number of other benefits can be identified. In general, using a series connection leads to higher currents and efficiency per die area, as well as results in a lower cost of the system compared with basic two-level topologies [92].

Yet, the series connection of active power semiconductor devices, i.e., transistors, especially SiC MOSFETs, is not trivially applicable. Mainly because of the issues with the uneven voltage sharing between the transistors in the stack, both in static and dynamic states, appearing due to several factors: differences in gate driver and power circuit layout between the stacked devices [93, 92]; the influence of parasitic capacitances [94]; or the imperfection and parameter variations, e.g., capacitance characteristics, in the SiC MOSFET devices themselves [95, 94]. Therefore, circuits based on the series connection of SiC MOSFETs require the inclusion of voltage balancing methods, leading to additional complexity in power converters [96].

There are several voltage compensation methods dedicated to series-connected transistors, identified for both conventional, slow-switching Si devices [97], as well as newer works on the rapid SiC MOSFETs [96, 98]. In general, these can be divided into two groups – passive and active methods.

When the passive voltage compensation methods are considered, simplicity is vital. As the name suggests, there are no active components, and the voltage is usually balanced by the means of external circuits connected to the transistor. A standout example could be the snubber circuit, i.e., a capacitor and a resistor (sometimes also with a diode) connected in parallel to each stacked transistor [97, 95]. Effectively, the increased output capacitance of the transistors slows down each device and minimizes the effects of natural mismatches, leading to a more even voltage distribution. However, the voltage is usually never fully balanced. While the method itself does induce any extra loss on the power devices themselves, the snubber circuit does add a substantial amount of extra losses, thus limiting the system's

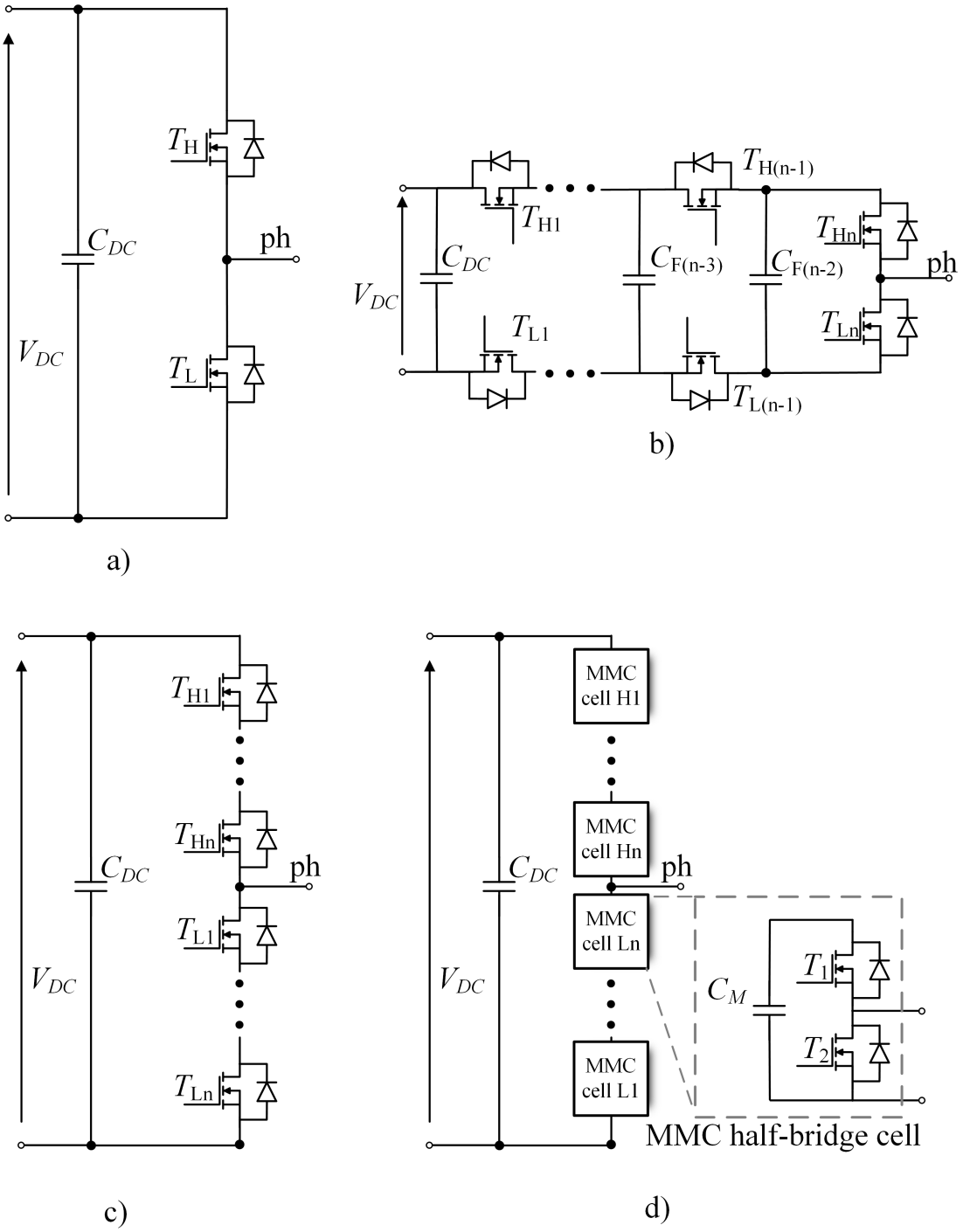

Figure 1.5: Generalized figure showcasing the possible methods to construct power converters in MV range: a) two-level topology with single power devices; b) classic multilevel topology (FC converter shown here); c) series connection of power transistors; d) MMC structure. Note that instead of a MOSFET, any power device can be applied as a switch for any of the topologies.

efficiency and adding components of considerable volume to the system. Nevertheless, the method is very simple and has proven to be a competent method for MV converters [99].

On the other hand, there are active voltage balancing methods based on closed-loop systems, minimizing the mismatches in the voltage based on the voltage measurements. While the general idea for the group is similar for each solution, the "actuator" deciding on the voltage distribution may differ. For example, in the active delay method [93], the voltage split is changed through minuscule delays added to specific transistors in the stack. Other approaches are based on extra current injection circuits [94] or other hardware-based techniques [100, 101]. Nevertheless, disregarding the type of active balancing, this group can be considered essentially lossless and can achieve near-equal voltage share. However, it comes with the cost of complicated circuitry and/or complex control, leading to an enlarged cost of the converters and possibly resulting in reliability issues in long-term operation.

In the end, the series connection of power transistors is a viable way to construct MV power converters. However, one must either accept simple snubber-based systems with additional power losses and lower power density or sophisticated, active circuits with no extra loss but with notably enlarged system complexity, e.g., through special control, additional measurements, or advanced gate drive circuits.

Another well-known solutions for creating MV power converters are the multilevel (ML) topologies. There is a vast array of different systems originating with cascaded topologies. Furthermore, considering only the most notable ones, neutral point clamped (NPC) [102] and its variations; the currently popular T-type converter [103, 104, 105]; the flying capacitor (FC) topology [106], depicted in Fig. 1.5b, and others [107] can be itemized. While there are several differences between the named topologies, a few general traits of conventional multilevel systems are distinguishable.

The main feature of multilevel converters is the concept of employing LV power devices to reach higher blocking voltages, similar to series connection systems. Although, here, the component structures are more advanced and employ other components in addition to the devices themselves, e.g., there are additional diodes in the NPC topology, or there are extra capacitors in the FC converters. Such complex circuits further necessitate the inclusion of more advanced modulation patterns when compared to two-level solutions.

In general, multilevel topologies are characterized by several advantages over two-level operated systems. The inclusion of more voltage levels in the output voltage provides the opportunity to improve the flexibility, achieve better recreation of sinusoidal currents, as well as bring lowered dv/dt ratio and EMI noise. Moreover, the power density can also be vastly improved, as the volume of the passive components, i.e., inductors, can be greatly

minimized [104]. On the other hand, the more voltage levels there are, the more complicated the structure and control become, as well as the system base cost increases – mainly because due to the need for voltage balancing. Nevertheless, multilevel systems are a popular choice for MV applications, especially in the lower voltage spectrum.

An important derivative of the multilevel converters is the MMC [108, 109, 110], introduced in 2001 and still widely investigated [111]. While it holds many similarities with the aforementioned, it is characterized by several attributes worthy of separate consideration. Most importantly, the main feature of the MMC is the modular aspect. Each leg of an MMC comprises many individual cells, usually identical ones. These cells can have different structures, e.g., as simple as the half-bridge cells depicted in Fig. 1.5d. Such a structure is especially beneficial for applications operating with notable voltages, where several or even tens of cells have to be employed, e.g., in HVdc systems [112, 113], but there are applications in the higher voltage spectrum of MV as well [108].

The inclusion of modularized, cell-based structures provides several vital aspects. First off, the reliability of MMC systems is high, as redundancy can be easily attained, and serviceability is improved as well [109]. Furthermore, the modular structure is beneficial in terms of system design, as the focus has to be put mainly on the cell, which is then multiplied. A similar approach is also seen for the control of the converter. Nevertheless, such a structure also is characterized by several drawbacks. For one, if a direct comparison with an FC system is considered, an MMC would exhibit at least twice the transistors assuming the same voltage level and also other components, i.e., capacitors. This also affects the size of the modules, which negatively impacts the switching loops, as well as the size of the whole system [114, 115]. All in all, regardless of the hindrances of MMCs, these are a common and noteworthy choice for elevated voltage applications in MV and HV ranges.

Finally, an emerging technique for the construction of MV power converters is the quasi-two-level (Q2L) approach. Originally, it was introduced as an alternative method of control for MMC systems that can drastically reduce the cell capacitance requirement at the cost of forgoing the multilevel aspect, as in a general scope, Q2L-controlled systems operate as conventional two-level systems [116, 117, 118, 119]. Furthermore, the method can also be effectively applied to FC converters [120, 121, 122]. The main difference in operation between Q2L and basic ML control methods is that in the former, the intermittent voltage levels are applied for a very brief time just to balance the voltages across the power devices, i.e., SiC MOSFETs, while in the latter, these are used for a notable amount of the switching period [123] – hence the difference is the energy stored in the capacitances.

Apart from the core difference resulting in intensively lowered volume of the capacitors,

as the stored energy can be reduced tenfold [119, 124], there are several other characteristics compared to conventional ML or MMC systems. The arm inductance requirement is immensely reduced, and the issue with circulating currents is nearly non-existent [125, 126]. Moreover, considering less severe capacitor voltage ripples, the closed-loop voltage balancing is also less challenging. On the other hand, the flexibility of shaping the output current is minimized; thus, higher inductance needs to be employed [119, 127].

Conventionally, the Q2L method was established with identical modulation patterns as in the conventional ML approach but with massively shortened intermittent levels. However, recently, there have also been presented concepts of employing the Q2L approach strictly to balance the voltages with the omission of the dv/dt ratio reduction, effectively deeming the alternate method equal to the approach with series-connected transistors [128, 129]. Thus, such implementation of Q2L control can be seen as a simpler alternative for more complex active voltage balancing methods, further considered in the publications included in the thesis. All in all, the Q2L method, in either form, is a notable method for MV power converters, recently gaining a lot of interest in academia and industry.

The general characteristics of the discussed approaches are summarized in Table 1.3. When the complexity is considered, the single device is definitely the most straightforward option, both in terms of control and system design, while MMC is characterized by a sophisticated structure and convoluted control. Since the cost of high-voltage-breakdown power devices is still quite enormous, solutions that employ several LV transistors are the most favorable here. Volume-wise, the single-device option can be, again, considered the best one. On the other hand, series-connection-based circuits with snubbers require notable volume, similar to the MMC systems. The situation is akin to the parasitics and the layout complexity. Because of the redundancy option, MMCs are favored in terms of reliability, while the lowest power losses can be achieved with the solutions employing simple structures with LV power devices – the actively balanced SC and Q2L systems. Finally, apart from the single device, two-level option, any method can theoretically reach any blocking voltage, but ML-MMC and Q2L-MMC would be the choice for notable voltage levels.

Considering all the mentioned methods and their characteristics, the approach for creating converter legs for MV applications is not a trivial endeavor. Depending on the end application, various traits may be seen as critical, and thus, a single, best option cannot be named in general. Furthermore, the situation becomes even more complicated as full converter topologies come into play, whether the system has to be ac-dc or dc-dc, have the insulation or not, if the structure has to be combined with other structures to ensure other features, e.g., soft-switching; and many more.

Table 1.3: Characterization of different methods for MV power conversion.

Parameter	Single device	SC - passive	SC - active	Q2L	ML	MMC
Complexity	low	medium	high	medium	medium	high
Cost	high	medium	medium	medium	high	high
Volume	low	high	medium	medium	medium	high
Parasitics	low	medium	medium	medium	medium	high
Reliability	medium	medium	low	low	medium	high
Efficiency	medium	low	high	high	high	medium
Blocking voltage	low	high	high	high	high	high

1.4 Motivation & aim

The main motivation behind the thesis is the constant advances in SiC-based power device technology that allow for more straightforward construction of high-performance medium voltage power electronics. Medium voltage power electronics have been widely analyzed and constructed for many years already, especially for high power systems, mainly since an increase in the voltage leads to lower current, which reduces the conduction power losses and further enables the lower volume of the connections, e.g., busbars and cables. However, until recently, medium voltage applications were bound only to Silicon devices, such as IGBTs, or IGCTs, since only these types of power devices could operate with breakdwon voltages higher than 1 kV. It is well known that these devices are characterized by many drawbacks, e.g., the tail current of IGBT, leading to relatively high power losses, the non-full controllability of the thyristors, or the high cost of IGCTs. Then, the introduction of SiC power devices brought the highly performing MOSFET into the MV range, with prototype devices at 10 kV breakdown voltages and higher. However, although SiC-based devices already allow for a substantial enhancement of MV converters over their Si-based counterparts, several issues constraining the appropriate utilization of Silicon Carbide still need to be addressed. The most important ones include: how to properly construct the hardware that allows for fast-switching operation, how to model the converters employing SiC-based semiconductor devices and accurately estimate the power losses, what topologies and control methods are the most efficient.

Thus, the aim of the dissertation was to study the possibilities of effective electric energy conversion in medium voltage range with power converters based on Silicon Carbide power devices.

Other, more specific goals can be established as parts of the core aim and are depicted

below.

- Methods to precisely characterize the output capacitance of MV SiC MOSFETs power devices allowing for accurate estimation of power losses based on simple experimental systems can be established.
- Methods to accurately estimate MV SiC device power losses within power converters based on simple experimental setups can be established.
- There are several converter topologies that can effectively utilize SiC power devices in medium voltage power electronic systems.
- Quasi-two-level method is a prominent method for creating SiC-based MV power converters.
- TCM-Q2L control technique allows the construction of high-efficient dc-dc SiC-based MV power converters operating at high frequency.
- Quasi-square-wave technique can be employed to achieve fully soft-switched operation of SiC power MOSFETs in MV range.

1.5 Publications included in the dissertation

The dissertation contains the following five publications, where the author is a co-creator:

[P1] J. Rąbkowski, M. Zdanowski, **R. Kopacz**, F. Gonzalez-Hernando, I. Villar and U. Larrañaga, "From the Measurement of COSS–VDS Characteristic to the Estimation of the Channel Current in Medium Voltage SiC MOSFET Power Modules," in IEEE Transactions on Instrumentation and Measurement, vol. 72, pp. 1-10, 2023, Points according to the Ministry of Education and Science: **100**, Impact Factor: **5.332**. Contribution of the dissertation author: **25%**. [130]

[P2] J. Rąbkowski, H. Skoneczny, **R. Kopacz**, P. Trochimiuk, G. Wrona, "A Simple Method to Validate Power Loss in Medium Voltage SiC MOSFETs and Schottky Diodes Operating in a Three-Phase Inverter", Energies, 13, 4773, 2020. Points according to the Ministry of Education and Science: **140**, Impact Factor: **3.252**. Contribution of the dissertation author: **25%**. [131]

[P3] P. Trochimiuk, **R. Kopacz**, K. Frąc and J. Rąbkowski, "Medium Voltage Power Switch in Silicon Carbide—A Comparative Study," in IEEE Access, vol. 10, pp. 26849-26858, 2022. Points according to the Ministry of Education and Science: **100**, Impact Factor: **3.476**. Contribution of the dissertation author: **40%**. [132]

[P4] **R. Kopacz**, M. Harasimczuk, P. Trochimiuk, G. Wrona and J. Rąbkowski, "Medium Voltage Flying Capacitor DC–DC Converter With High-Frequency TCM-Q2L Control," in IEEE Transactions on Power Electronics, vol. 37, no. 4, pp. 4233-4248, April 2022. Points according to the Ministry of Education and Science: **200**, Impact Factor: **5.967**. Contribution of the dissertation author: **40%**. [129]

[P5] **R. Kopacz**, M. Harasimczuk, P. Trochimiuk and J. Rąbkowski, "Investigation of Soft-Switching QSW Technique in DC/DC SiC-Based Flying Capacitor Converter With Q2L Control," in IEEE Transactions on Industrial Electronics, vol. 70, no. 9, pp. 9035-9045, Sept. 2023. Points according to the Ministry of Education and Science: **200**, Impact Factor: **8.162**. Contribution of the dissertation author: **50%**. [133]

The summarized bibliometric parameters for the core publications [P1]-[P5] are depicted in Table 1.4.

Table 1.4: Summary of the parameters of the core publications included in the dissertation.

Summarized for [P1]-[P5]	
Points according to the Ministry of Education and Science	Impact Factor
740	26.189

1.6 Other achievements

Besides the mentioned publications, core for the dissertation, the author has also contributed to several other publications (5 journal papers, 9 conference proceedings), closely related to the subject of the thesis.

Journal publications:

[J1] J. Rąbkowski, **R. Kopacz**, "Extended T-type inverter", in Power Electronics and Drives, vol.3, no.1, 3918, pp.55-64. Points according to the Ministry of Education and Science: **20**, Impact Factor: **N/A**. Contribution of the dissertation author: **30%**. [134]

[J2] B. Lasek P. Trochimiuk, **R. Kopacz**, and J. Rąbkowski, "Parasitic-based active gate driver improving the turn-on process of 1.7 kV SiC power MOSFET", in Applied Sciences, 2021, 11, 2210. Points according to the Ministry of Education and Science: **100**, Impact Factor: **2.7**. Contribution of the dissertation author: **15%**. [135]

[J3] P. Trochimiuk, **R. Kopacz**, G. Wrona and J. Rąbkowski, "Active Voltage Balancing of Series-Connected 1.7 kV/325 A SiC MOSFETs Enabling Continuous Operation at Medium Voltage," in IEEE Access, vol. 9, pp. 8604-8614, 2021. Points according to the Ministry of Education and Science: **100**, Impact Factor: **3.476**. Contribution of the dissertation author: **30%**. [93]

[J4] **R. Kopacz**; M. Harasimczuk, B. Lasek, R. Miśkiewicz, and J. Rąbkowski, "All-SiC ANPC Submodule for an Advanced 1.5 kV EV Charging System under Various Modulation Methods", Energies 2021, 14, 5580. Points according to the Ministry of Education and Science: **140**, Impact Factor: **3.252**. Contribution of the dissertation author: **40%**. [136]

[J5] **R. Kopacz**, M. Harasimczuk, J. Rabkowski, R. Sobieski, "Three-Level Interleaved Non-isolated DC/DC Converter as a Battery Interface in an EV Charging System with Bipolar DC-Link", Przegląd Elektrotechinczny, vol. 5, 2023. Points according to the Ministry of Education and Science: **70**, Impact Factor: **N/A**. Contribution of the dissertation author: **55%**. [107]

Conference proceedings:

[C1] **R. Kopacz**, D. Peftitsis and J. Rabkowski, "Experimental study on fast-switching series-connected SiC MOSFETs," European Conference on Power Electronics and Applications (EPE'17 ECCE Europe), Warsaw, Poland, 2017, pp. P.1-P.10. Contribution of the dissertation author: **50%**. [95]

[C2] J. Rabkowski, S. Piasecki, and **R. Kopacz**, "An extended T-type (eT) inverter based on SiC power devices", European Conference on Power Electronics and Applications (EPE'18 ECCE Europe), Riga, Latvia, 2018, pp. P.1-P.10. Contribution of the dissertation author: **20%**. [134]

[C3] P. Trochimiuk, **R. Kopacz**, G. Wrona and J. Rąbkowski, "Medium voltage power switch based on 1.7 kV SiC MOSFETs connected in series inside power modules," European Conference on Power Electronics and Applications (EPE '19 ECCE Europe), Genova, Italy, 2019, pp. P.1-P.10. Contribution of the dissertation author: **25%**. [98]

[C4] **R. Kopacz**, P. Trochimiuk, G. Wrona and J. Rąbkowski, "High-frequency SiC-based medium voltage quasi-2-level flying capacitor DC/DC converter with zero voltage switching", European Conference on Power Electronics and Applications (EPE '20 ECCE Europe), Lyon, France, 2020, pp. P.1-P.10. Contribution of the dissertation author: **50%**. [122]

[C5] J. Rabkowski, D. Peftitsis, R. Sobieski, M. Harasimczuk, R. Miśkiewicz, K. N. Kumar, **R. Kopacz**, K. Kalinowski, and P. Trochimiuk, "Advanced charging system with bipolar DC-link and energy storage",2022 Progress in Applied Electrical Engineering (PAEE), Koscielisko, Poland, 2022, pp. 1-6. Contribution of the dissertation author: **10%**. [137]

[C6] M. Harasimczuk, K. Kalinowski, R. Miskiewicz, **R. Kopacz**, B. Lasek and J. Rabkowski, "Three-Level ANPC Converter as an Input Stage of an EV Charging System with Bipolar DC Link," PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2022, pp. 1-6. Contribution of the dissertation author: **10%**. [138]

[C7] J. Rąbkowski, **R. Kopacz**, R. Sobieski, M. Zdanowski, P. Trochimiuk and S. Piasecki, "Continuous operation of medium voltage SiC power modules in the test circuit," 2022 Progress in Applied Electrical Engineering (PAEE), Koscielisko, Poland, 2022, pp. 1-6. Contribution of the dissertation author: **30%**. [139]

[C8] R. Sobieski, R. Miskiewicz, J. Rabkowski and **R. Kopacz**, "Two-phase interleaved DC-DC converter with 3.3 kV SiC MOSFET modules," 2023 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC), Venice, Italy, 2023, pp. 1-5. Contribution of the dissertation author: **10%**. [89]

[C9] **R. Kopacz**, M. Harasimczuk J. Rabkowski and R. Sobieski, "Experimental evaluation of inductor configurations and modulation techniques in an interleaved three-level DC/DC SiC-based converter," 2023 IEEE 17th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), Talinn, Estonia, 2023, pp. 1-6. Contribution of the dissertation author: **50%**. [140]

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Chapter 2

Contribution

In this Chapter, the contribution of the dissertation author in the scope of advances in SiC-based medium voltage power converters is presented on the basis of the publications included in the thesis.

2.1 Modeling of medium voltage SiC power devices & converters

While the many aspects of SiC power devices, especially SiC MOSFETs, can be directly derived from their Si counterparts, there are numerous crucial differences related to the material properties and the devices' internal structure, as well as the associated device packaging that necessitate further studies to fully utilize SiC-based transistors in MV power electronic applications. Namely, there are concerns regarding the phenomena behind the switching of the SiC MOSFET, e.g., the turning-off process – crucial for the soft-switched power converters employing ZVS techniques. Therefore, proper modeling, characterization, and measurement of the devices are essential to determine the behavior of the devices, estimate the power losses, and thus properly design the converters to achieve highly efficient and compact MV power electronics.

2.1.1 From the measurement of COSS-VDS characteristic to the estimation of the channel current in medium voltage SiC MOSFET power modules [P1]

The introduction of SiC MOSFETs capable of blocking several kV allows for the construction of MV power converters with lower losses and higher power density compared to conventional ones based on Si IGBTs, also for ZVS-operated circuits, e.g., dc-dc convert-

ers or inductive power transfer systems. In such circuits, the switching loss at turn-on is nearly fully eliminated, for example, as in TCM-operated converters [141]. Thus, the turn-off losses, even though relatively lower than the turn-on ones, become a substantial part of total converter losses, and their proper determination is vital for the proper design of power converters from the electro-thermal perspective, i.e., the heat-sink. Therefore, in order to be able to construct competitive converters in the MV range, a simple and accurate method to obtain the turn-off power loss is necessary.

In general, the switching-off behavior of state-of-the-art SiC MOSFETs is complex and has yet to be fully described [142, 143]. However, the basic consensus is that the measured drain current is split between the lossy MOSFET channel current and nearly lossless capacitive current [144]. Thus, there is a need to correctly differentiate between the two current parts, which can be done through the $C_{OSS} - V_{DS}$ characteristic of the device. Unfortunately, this characteristic is not always provided by the manufacturer, especially for devices still under development, which is often the case for new SiC MOSFET power modules. The situation is even more complicated as for modules rated at several hundred amperes, the devices comprise several paralleled chips. Yet, from the designer's perspective, a power module is still a single device, and thus, a simple $C_{OSS} - V_{DS}$ characterization method is needed.

While there are several methods to determine $C_{OSS} - V_{DS}$ characteristic, they are complex and require expensive equipment, additional circuitry, or sophisticated calibration [145, 146]. Thus, in the paper, a novel method for characterization, based on a simple setup akin to conventional circuits used for single- and double-pulse tests, is proposed and validated through an experimental study using a 1700-V/900-A SiC MOSFET power module, which allows for improving the precision of power losses estimation of soft-switched dc–dc converters – helpful in enhancing the design process of highly efficient, compact, high-power converters in MV applications.

The summarized contribution of the publication is listed below:

- short overview of characterization methods for SiC MOSFETs;
- description of the SiC MOSFET internal structure, with a focus on the output capacitance in power modules;
- proposal of a novel, simple method to obtain $C_{OSS} - V_{DS}$ characteristic for MV SiC MOSFETs, also in power module configuration;
- study of the effect of nonzero turn-off voltage on the $C_{OSS} - V_{DS}$ characteristic;
- determination of the channel current using the obtained $C_{OSS} - V_{DS}$ characteristic;

- establishing the importance of the utilization of the split between the capacitive and channel currents for the estimation of switching loss in soft-switched converters;
- design and construction of an MV test bench for the experiments;
- validation of the proposed concept using a 1700-V/900-A SiC MOSFET power module.

The specific contribution of the dissertation author for the publication:

- performing the literature overview on SiC MOSFET capacitances and their characterization methods;
- design & construction of the control part of the experimental setup;
- participating in the experimental study;
- analysis, processing of data, validation of the results;
- preparation of the paper, initial draft, and final version; leading the submission and review process (corresponding author).

2.1.2 A Simple Method to Validate Power Loss in Medium Voltage SiC MOSFETs and Schottky Diodes Operating in a Three-Phase Inverter [P2]

SiC MOSFETs have been successfully introduced for MV power converters as superior alternatives for Si IGBTs, as they provide faster switching speeds and lower turn-on and turn-off losses but are not necessarily favorable in terms of on-state performance [147]. Furthermore, there have been several works presented investigating MV-rated inverters, also employing SiC MOSFETs [39, 148]. However, as the MOSFETs are capable of conducting reverse currents, the relations between current and loss split in transistor-diode pairs are much different, and thus the considerations from prior work are not directly applicable here. Thus, a thorough analytical study on the semiconductor power losses in inverters is presented in the paper, focusing on a case with a SiC MOSFET-Schottky pair.

Moreover, when the complex process of medium-voltage power converter design is considered, along with the electro-thermal aspects, datasheet values are often not sufficient. Additionally, the well-known double-pulse testing is also sometimes considered for the validation of the device's performance. However, the design, and thus the outcomes of the

testing, can vary between the tests and the final system, as the distribution of the parasitics, highly affecting the switching performance, differs [149]. Therefore, there is a great need for a new, low-cost, and simple method of experimental evaluation of MV SiC MOSFET power modules.

There have been several methods presented in the literature [52]. The issue is especially complex for the new wide-band gap power devices, where the generated EMI and low value of losses to be measured are the sources of challenge. In general, there are several methods to determine the power losses [73], electrical-based, and calorimetric-based [75]. However, each requires expensive and sophisticated setups, which is further accentuated as the voltage and current levels for MV applications are high. Thus, a novel, straightforward method to emulate the power losses of MV power converters using a simple half-bridge setup and conventional low-power supply is proposed in the paper.

The summarized contribution of the publication is listed below:

- a brief overview of methods for estimating power losses in SiC-based MV power converters;
- a thorough study of power loss estimation in an exemplary, common case for MV power converters – a two-level inverter;
- a detailed description of the phenomenon of current sharing between the SiC MOSFET channel and the body diode with its effect on power loss, including thorough theoretical analysis;
- proposal of a novel, straightforward method to estimate on-state power losses of a SiC power module based on emulation procedure through a simple hardware setup converged with a MATLAB script, using only minimal power requirement (2 kW supplied for a studied 220 kVA inverter);
- design and construction of a half-bridge experimental setup;
- experimental validation using a half-bridge circuit with 3.3 kV/450 A SiC MOSFET modules.

The specific contribution of the dissertation author for the publication:

- design & construction of the control part of the experimental setup;
- participating in the experimental study;

- analysis, processing of data, validation of the results;
- preparation of the paper, initial version, final version.

2.2 Topology concepts for MV power converters

As aforementioned, there are a number of approaches for constructing SiC-based power converters in the MV range. Thus, this Section presents an experiments-enhanced review paper of the most prominent methods.

2.2.1 Medium Voltage Power Switch in Silicon Carbide—A Comparative Study [P3]

The introduction of high voltage-rated WBG devices allows for easier construction of MV power converters. SiC MOSFETs reach the blocking voltage levels previously available only for Si IGBTs, leading to lower power losses, higher operating frequencies, and more. Simultaneously, at the lower spectrum of voltages, SiC power devices can be directly applicable in two-level topologies instead of complex structures. On the other hand, SiC devices are not always the superior choice [78]. Also, the cost of the emerging WBG technology is very high. Thus, there is a need to further analyze the possibilities in order to establish the advantages and disadvantages of each approach.

The possible methods for MV power converters include the employment of single MV devices rated at several kVs and higher, using a simple two-level topology [40, 88, 87]; series connection of LV SiC MOSFETs, with either passive or active voltage balancing [94, 97, 93]; conventional multilevel approach, e.g., using FC topology [106]; or employing the emerging Q2L control to converge the traits of series-connection circuit using a multilevel topology [116, 128, 129]. While these have been separately described in the literature quite expansively, a thorough comparative study performed for identical conditions for each method was lacking.

To this end, in the paper, the mentioned methods are theoretically and experimentally compared, including insights on power loss, gate drivers, circuit and design complexity, cooling, reliability, cost, and more, at up to 300 A rms and 1.5 kV. The insights can be effectively used as a guideline for designers seeking appropriate topology for a specific MV application.

The summarized contribution of the publication is listed below:

- an overview of methods to create MV power converters employing state-of-the-art SiC

MOSFETs, including single high-voltage power devices, series connection, multilevel approach, and the quasi-two-level method;

- design and construction of an MV prototype for each of the methods;
- experimental validation and comparison for each of the studied concepts at up to 1.5 kV and 300 A rms current;
- a power loss experimental study for each method;
- a detailed analysis of advantages and disadvantages of each method, considering efficiency, gate drivers, circuit complexity, cooling, reliability, cost, and more.

The specific contribution of the dissertation author for the publication:

- performing the literature overview on various methods for the realization of SiC power devices in MV power converters;
- design & construction of the experimental setup regarding the multilevel and quasi-two-level operation, and the controller of the system;
- participating in the experimental study;
- analysis, processing of data, validation of the results;
- preparation of the paper, initial draft, and final version.

2.3 MV SiC-based dc-dc converters

Dc-dc converters, now commonly employing SiC power semiconductor devices, are widely used in the MV range, spanning from battery storage and microgrid systems through RES circuits, as well as traction and e-mobility applications, and many more. Therefore, in this Section, an exemplary case of a new MV non-isolated, bidirectional, soft-switching dc-dc converter employing state-of-the-art SiC MOSFETs that can be employed in dc microgrids as an auxiliary traction converter or in battery energy storage and PV applications, is considered. The proposed novel concepts for both circuit arrangement and control, supported by a detailed theoretical analysis and discussion in regard to the literature and validated experimentally, are established as a highly competitive option for dc-dc power conversion in MV applications.

2.3.1 Medium voltage flying capacitor dc–dc converter with high-frequency tcm-q2l control [P4]

With the introduction of WBG power devices, MV power converters flourish, as highly-performant SiC MOSFETs with high blocking voltages are already widely available and are still being further developed. Therefore, many formerly LV applications have their voltages extended to MV territory, e.g., battery energy storages or PV strings [7]. Furthermore, other MV applications, i.e., traction systems, can also significantly benefit from the inclusion of SiC power devices into their designs. This necessitates the construction of low-loss and low-cost MV dc-dc power converters.

As was elaborated on in the previous Section, there are several approaches for the employment of SiC transistors to create MV power converters [132]. Furthermore, a vast array of possibilities to construct bidirectional dc-dc converters, also with soft-switching behavior, is available [150]. For example, multilevel [151, 152], switched capacitor [153], or interleaved [154] topologies can be named.

In the paper, a novel MV non-isolated, bidirectional, soft-switching dc-dc converter employing state-of-the-art SiC MOSFETs is proposed. The system is based on a conventional FC topology, employing four power switches rated at a voltage lower than the dc-link voltage, with the new TCM-Q2L control, based on the convergence of quasi-two-level control [116, 117, 128] enabling the use of LV SiC MOSFETs for the MV system with minimized capacitor volume, and the TCM approach to ensure ZVS at turn-on at a wide voltage gain and load range [152], leading to high-frequency operation. The concept is validated via an experimental model tested up to 250 kHz switching frequency, 1.5 kV, and 10 kW of power, and a thorough theoretical description of the operating modes, including a detailed mathematical analysis, is given. It is shown that the proposed converter can be effectively and competitively employed for MV dc-dc power conversion, as it provides exceptional efficiency (up to 99.1%) and a compact footprint.

The summarized contribution of the publication is listed below:

- a short review of methods for the realization of SiC-based dc-dc non-isolated bidirectional converters in MV range;
- proposing a novel TCM-Q2L control concept for highly efficient and compact dc-dc non-isolated converter employing SiC MOSFETs with soft-switching;
- proposing a new method for voltage balancing in Q2L dc-dc converters;

- a thorough theoretical description of the TCM operation of the converter, also including the resonant behavior;
- an advanced simulation of the proposed converter in Saber software;
- design and construction of an MV prototype of the proposed converter;
- validation of the proposed converter at up to 1.5 kV and 10 kW of power with a peak efficiency of 99.1%;
- a detailed comparison with other state-of-the-art concepts for dc-dc non-isolated converters, deeming the proposed system highly competitive.

The specific contribution of the dissertation author for the publication:

- proposing a novel TCM-Q2L control concept for highly efficient and compact dc-dc non-isolated converter employing SiC MOSFETs with soft-switching;
- proposing a new method for voltage balancing in Q2L dc-dc converters;
- participating in the theoretical analysis for the proposed system;
- performing the literature overview on various methods for the realization of SiC-based dc-dc non-isolated converters in MV range, with a thorough comparison to other state-of-the-art concepts;
- preparing the simulation models and performing the simulation study;
- design & construction of the whole converter and the experimental setup;
- leading the experimental study;
- analysis, processing of data, validation of the results;
- preparation of the paper, initial draft, and final version; leading the submission and review process (corresponding author).

2.3.2 Investigation of soft-switching QSW technique in DC/DC SiC-based flying capacitor converter with Q2L control [P5]

The paper is a direct follow-up to the previous article, extending the proposed converter to achieve full soft-switching, also at turn-off, and further improving the efficiency by a marginal cost in power density.

Apart from the aforementioned concerns regarding MV dc-dc converters, the introduction of SiC MOSFET is a challenging task, mainly due to their exceptional switching speeds and high voltage ratings, which lead to notable dv/dt ratios. These, in convergence with the unavoidable parasitics in the circuits, are the source of several substantial issues. To name a few, increased voltage overshoots, enlarged power losses, and higher EMI generation are the crucial ones [30, 34]. A viable solution to mitigate this issue is either slowing down the transistors or employing supplementary dv/dt limiting circuits [85, 55]. However, such an approach is burdened with increased complexity and volume.

Furthermore, a vast number of methods to establish full soft-switching have been investigated [155, 156], providing the possibility to maximize the power density while maintaining low losses. A conventional approach would be to employ resonant [157, 158] or quasi-resonant [159] cells. However, these necessitate the addition of several extra components, leading to lower power density and increased cost. Furthermore, they are usually bound to a specific operating point, exhibiting exceptional performance only at a narrow operating range. Another method to achieve soft-switching is based on ZVT topologies [160, 161]. Unfortunately, this approach also requires adding extra components, e.g., active snubber cells. Finally, there are converters based on TCM (also referred to as QSW) [162, 152], which incorporate the filter inductor as a part of the resonant circuit, maximizing the power density. On the other hand, ZVS is only assured at turn-on. Thus, the obtained efficiencies are somewhat limited.

In the paper, a simple, low-volume method to ensure full soft-switching and minimize the harmful dv/dt transistors' ratio is proposed. Based on the TCM-Q2L system [129], with the addition of small capacitors in parallel to each transistor, a fully soft-switched, ultra-low power loss MV dc/dc converter based on SiC MOSFETs is shown. The experimental prototype is validated at up to 1.5 kV and 15 kW, reaching a peak efficiency of 99.5%. It is exhibited that the proposed converter enables full utilization of SiC power devices' possibilities and can be effectively used in MV dc-dc applications, surpassing its' counterparts.

The summarized contribution of the publication is listed below:

- a brief overview of methods for the realization of fully soft-switched SiC-based dc-dc non-isolated converters in MV range;
- proposing a novel concept of the utilization of small capacitors in parallel to the SiC MOSFETs to lower the switching losses following the quasi-square-wave techniques, so the efficiency of the dc-dc converter is maximized, and the dv/dt ratio is reduced
- a thorough theoretical analysis of the proposed converter with the additional resonant

capacitors, including a study on power loss distribution across the converter components;

- establishing design guidelines for the auxiliary capacitor selection to allow full utilization of SiC MOSFETs in MV dc-dc converters
- design and construction of an MV prototype of the proposed converter;
- validation of the proposed converter at up to 1.5 kV and 15 kW of power with a maximum efficiency of 99.5%;
- a detailed comparison with other state-of-the-art concepts for soft-switched dc-dc non-isolated converters, establishing the proposed system as a top choice for efficient MV dc-dc power conversion;

The specific contribution of the dissertation author for the publication:

- proposing a novel concept of the utilization of small capacitors in parallel to the SiC MOSFETs to lower the switching losses following the quasi-square-wave techniques, so the efficiency of the dc-dc converter is maximized, and the dv/dt ratio is reduced;
- participating in the theoretical analysis for the proposed system;
- performing the literature overview on various methods for the realization of soft-switching techniques in dc-dc converters in MV range, with a thorough comparison to other state-of-the-art concepts;
- preparing the simulation models and performing the simulation study;
- design & construction of the whole converter and the experimental setup;
- leading the experimental study;
- analysis, processing of data, validation of the results;
- preparation of the paper, initial draft, and final version; leading the submission and review process (corresponding author).

Chapter 3

Publications

The dissertation contains the following five publications, where the author is a co-creator:

3.1 From the measurement of COSS-VDS characteristic to the estimation of the channel current in medium voltage SiC MOSFET power modules [P1]

[P1] J. Rąbkowski, M. Zdanowski, **R. Kopacz**, F. Gonzalez-Hernando, I. Villar and U. Larrañaga, "From the Measurement of COSS–VDS Characteristic to the Estimation of the Channel Current in Medium Voltage SiC MOSFET Power Modules," in IEEE Transactions on Instrumentation and Measurement, vol. 72, pp. 1-10, 2023, Points according to the Ministry of Education and Science: **100**, Impact Factor: **5.332**. Contribution of the dissertation author: **25%**. [130]

From the Measurement of C_{OSS}–V_{DS} Characteristic to the Estimation of the Channel Current in Medium Voltage SiC MOSFET Power Modules

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***Abstract*— This article presents a novel method for the dynamic measurement of C_{OSS}–V_{DS} characteristic of SiC MOSFET power modules based on the process of charging the output capacitance of the transistors. This technique has been used to determine the C_{OSS}–V_{DS} characteristics of medium voltage SiC MOSFET modules, which allows for the extraction of the capacitive current while switching off the transistor. Based on this measurement method, the influence of the turn-off gate voltage V_{GS-OFF} on the C_{OSS}–V_{DS} characteristics has been studied, exhibiting an impact on the output capacitance at low drain–source voltages. However, it is shown that the effect of V_{GS-OFF} on the capacitive current and power loss is limited in this area. Finally, the channel current and the capacitive current distribution within the drain current were determined based on the determined C_{OSS}–V_{DS} in the experimental test at various switched currents and switching speeds. According to the capacitive charge calculations for several cases, the method's accuracy is high enough to perform switching power loss estimations for medium voltage power modules to be employed in the design of the state-of-the-art power converters. Furthermore, the method is very simple, based on basic capacitance equations, and the required experimental setup is very similar to one used in double-pulse tests.**

***Index Terms*— Dynamic characterization, MOSFET, power electronics, silicon carbide, switching losses, zero-voltage switching.**

I. Introduction

MEDIUM voltage SiC MOSFETs are excellent candidates for high-power soft-switched power converters, where they can replace currently employed Si-based IGBTs. Operating in zero voltage switching (ZVS) conditions, such as in dc–dc or inductive power transfer (IPT) converters, these power semiconductors can achieve lower power losses, improving the overall efficiency of the system [1], [2], [3], [4]. Such systems usually operate at high switching frequencies, and a substantial part of the power losses occurring in semiconductor elements is losses generated during the switching-off process. Therefore, it is essential to correctly determine the switching losses to design the converter properly from an electrothermal perspective. Several publications, to mention only [5], [6], [7], [8], [9], and [10], have shown that the switch-off transition is quite complex and has not been fully examined yet. This is especially true for SiC MOSFETs, which switch at exceptional speeds, showcasing the issues that were omittable in the case of slow Si counterparts [5], [6]. For example, using SiC-based power devices with sufficient gate current may even lead to a situation with ultralow turn-off switching losses [7], and thus considering the gate driver is essential as well [8]. Moreover, apart from the commonly used power loss sources in the form of switching and conduction losses, additional losses such as residual loss [9] should also be taken into account. Finally, the effects of the measuring equipment have a substantial impact as well [10]. All in all, without deep analysis of the turn-off switching process, it can be concluded that the drain current includes the channel current, which causes conduction power losses in the transistor's channel, and the capacitive current, which is almost lossless [11]. Therefore, to correctly determine the switch-off power losses, it is necessary to distinguish these two components. This can be done by finding the capacitive current from the derivative of the drain–source voltage; for this, the C_{OSS}–V_{DS} characteristic of the power device must be employed [12]. However, this characteristic is not available for all power modules—this is the case of the power modules discussed in this work [13], [14], [15] or other power modules under development. Moreover, the characteristics provided by the manufacturer are usually measured only for gate–source voltage $V_{GS} = 0$, while gate-related capacitance is dependent on polarization, as has been proved both in TCAD simulations and experimentally [16], [17], [18].

The problem of characterization of MOSFET parameters [19], [20], including measuring C_{OSS}–V_{DS} characteristics, also for SiC power devices, was undertaken by many research teams [16], [17], [18], [19], [20], [21], [22], [23], [24], [25], [26]. The key question is if the observations for single-chip modules will be the same as for multichip power modules.

There are classic methods using an impedance analyzer or an *LRC* bridge to determine the C_{OSS}–V_{DS} characteristics, but

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the main problem is the need for high-voltage polarization, as most of the equipment is not able to reach even 800 V, not to mention higher voltages required for testing medium voltage power modules. Hence, various circuit concepts have arisen to allow measurements at higher voltages [16], [17], [18], [21]; however, the complexity of such systems is high. Another testing approach is based on running one- or two-pulse tests and observing the corresponding waveforms to determine the charges and capacitances [22], [23], [24], [25]. It is also possible to use a similar method in transistors' continuous operation without load [26]. However, these methods also induce their complexities, such as the need for another active switch in parallel to the device under the test [22], which may induce additional error; or the requirement of precise calibration of the inductor to achieve the resonance with C_{OSS} capacitance [23]; or were focused on other transistor capacitances, e.g., C_{RSS} [24], [25].

Considering the special features of medium voltage SiC power modules, i.e., a large active surface and potentially a large output capacitance, the authors propose a very simple, dynamic method for the measurement of C_{OSS} capacitance based on a single-pulse test. It is based on monitoring the drain–source voltage and the current flowing through the power device. The method has been successfully validated, showing that it is possible to precisely determine the C_{OSS}–V_{DS} characteristic without much computational and experimental effort, based on basic capacitance equations and using a simple setup akin to the conventional double-pulse test bench. This method has also been employed to study the influence of the turn-off gate voltage $V_{\mathrm{GS-OFF}}$, whose value affects the parasitic capacitances of the power device.

This article is organized as follows: after the introduction, the origins of the parasitic capacitances in a SiC MOSFET device are briefly described, and then, the proposed method for measuring the C_{OSS}–V_{DS} characteristic is presented. In Section III, this method is applied to a 1700-V/900-A SiC MOSFET power module to find suitable characteristics, also with nonzero gate polarization. Then, the studied devices are tested in single-pulse tests with an inductive load at different switched currents and switching speeds, with frequencies up to 25 kHz, and the capacitive current is estimated based on the determined C_{OSS}–V_{DS} characteristic. The work is concluded with a discussion of the results and a summary of the primary outcomes, successfully validating the proposed method.

This article is an extension of the proceedings article [12], but with additional theoretical insight, a more detailed description of the proposed method, as well as an expanded experimental study, also including the impact of different turn-off V_{GS} values.

II. Origins of the SiC MOSFET Output Capacitance

A. Single-Cell MOSFET Capacitances

The origins of parasitic capacitances of SiC vertical drift region-type double-diffusion MOSFET (VDMOS) are directly associated with the internal structure of the power semiconductor device. Depending on the gate-to-source voltage V_{GS} and if it is below or above the threshold voltage V_{TH}, two different

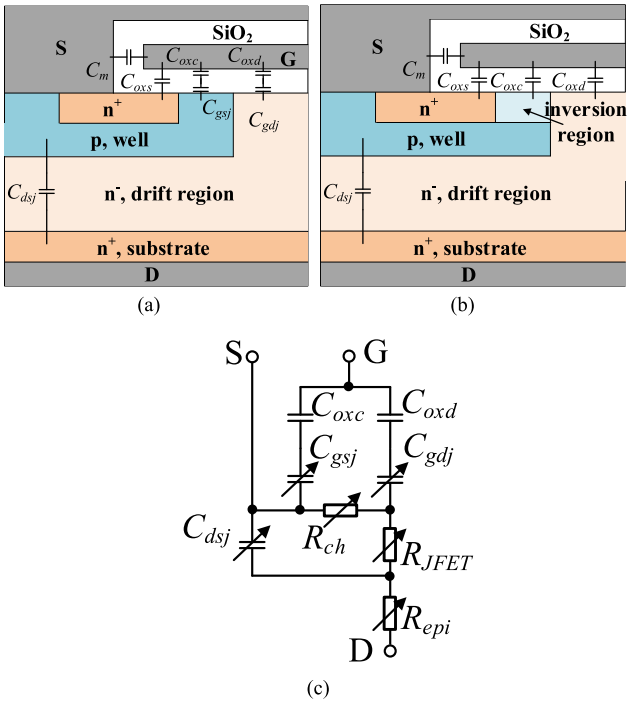

Fig. 1. Parasitic capacitances of a half-cell MOSFET structure-cross section with (a) closed ($V_{\mathrm{GS}} < V_{\mathrm{TH}}$) and (b) open ($V_{\mathrm{GS}} > V_{\mathrm{TH}}$) channel. (c) Equivalent electrical circuit of the transistor, including resistances for the current flow path [29].

situations can be distinguished. These situations are depicted in the cross-sectional illustrations of a MOSFET cell when the device is closed with $V_{\mathrm{GS}} < V_{\mathrm{TH}}$ in Fig. 1(a) and when the device is open ($V_{\mathrm{GS}} > V_{\mathrm{TH}}$) in Fig. 1(b) [19], [27], [28], [29], [30]. Furthermore, an equivalent electrical circuit of the transistor, also including the most relevant ON-state resistances (channel resistance R_{ch}, JFET region resistance R_{JFET}, and epitaxial layer resistance R_{epi}) for the current flow path, is shown in Fig. 1(c). Regarding the parasitic capacitances, the main difference between both situations is that while gate–source and gate–drain capacitances are separated by a depleted region in the p-well when the device is closed ($V_{\mathrm{GS}} < V_{\mathrm{TH}}$), they are connected through the channel resistance when the device is open [29].

Generally, the terminal parasitic capacitances between the following MOSFET electrodes are distinguished: gate-to-source capacitance C_{GS}, gate-to-drain capacitance C_{GD}, and drain-to-source capacitance C_{DS}. They are crucial in affecting the device switching behavior and are typically classified into three equivalent capacitances used for performance evaluation of the MOSFETs: the input capacitance seen from the gate ($C_{\mathrm{ISS}} = C_{\mathrm{GS}} + C_{\mathrm{GD}}$), the reverse transfer capacitance ($C_{\mathrm{RSS}} = C_{\mathrm{GD}}$), and the main interest of this article, the output capacitance seen from the drain ($C_{\mathrm{OSS}} = C_{\mathrm{DS}} + C_{\mathrm{GD}}$). The nature of the terminal capacitances is an effect of the device structure, including the semiconductor and oxide junctions and interfaces, and is highly dependent on V_{GS} and V_{DS} transistor voltages.

When a situation with a closed MOSFET channel is considered [Fig. 1(a)], the C_{GS} capacitance is comprised of the capacitance between the gate (G) and source (S) electrodes

within the oxide (C_m) and capacitances between the gate and: n^+ region (C_{oxs}), p^+ region (C_{oxc}), and p^+ depletion region (C_{gsj}). The capacitances between the gate and the drain (D) within the oxide C_{oxd} and the capacitance of the depletion region C_{gdj} are parts of the C_{GD} capacitance. Finally, the C_{dsj} capacitance across the depletion region below the p base is the only component of C_{DS}. When the gate polarization changes and $V_{GS} > V_{TH}$, which is the case during the turn-on process, the channel is established, and R_{CH} decreases [Fig. 1(b)]. Thus, the depletion capacitance C_{gsj} basically disappears, and capacitance C_{gdj} becomes negligible, while the oxide capacitances (C_m, C_{oxs}, C_{oxc}, and C_{oxd}) and the C_{dsj} capacitance remain, in practice, unchanged. Furthermore, when the device is open ($V_{GS} > V_{TH}$), the channel resistance is low, and therefore, $C_{oxc}+C_{gsj}$ is in parallel with $C_{oxd}+C_{gdj}$; hence, C_{GD} becomes part of C_{GS}.

On the other hand, when the device is turning-off, the increase of V_{DS} shifts the charge on the p-/n-junction, changing the C_{dsj} capacitance. Moreover, a similar effect is observed in the JFET region and C_{gdj}—both capacitances decrease with the drain potential.

Moreover, additional effects, such as drain-induced barrier lowering (DIBL) [31], are also observed, but they have a limited impact on the capacitance characteristics. Recently, the charge trap issues have also been discussed [32]; however, its influence is rather seen in the C_{GS} capacitance without affecting the C_{OSS} analyzed in this article.

B. MOSFET Capacitances in Power Modules

When high-power systems are considered, also in the medium voltage range, power module MOSFET packaging comes into play. Since these devices are made for high-power applications, current ratings of hundreds of amps are expected, requiring the use of multichip structures. In such modules, several MOSFET dies are connected in parallel and act as a single transistor, as shown in a simplified schematic of the power module in Fig. 2. This way, the power density achievable with these power modules can be improved since more power can be managed in a lower volume.

When multichip SiC power modules are considered, the characterization of the parasitic capacitances becomes even more complex as additional parasitics are present [33]. The complexity of employing SiC-based power modules is alleviated even more by the fact that, in most cases, the manufacturer does not share how many dies are used and what are the individual chips employed in the module, and generally, the datasheets lack of information regarding the parasitic capacitance characterization. Consequently, determining the switching performance of the SiC power modules based on capacitance characteristics is not a simple task and has not been studied widely before.

Furthermore, each MOSFET chip in a power module is characterized by different values of, among others, internal gate resistances and capacitances. Thus, in practice, the switching process for each chip occurs individually and can vary between the paralleled wafers. However, from the power electronics designer's perspective, the power module is still a single device and a characterization method based on establishing an equivalent characteristic seen from the power device terminals is required. To this end, such a technique is proposed in Section III of this article.

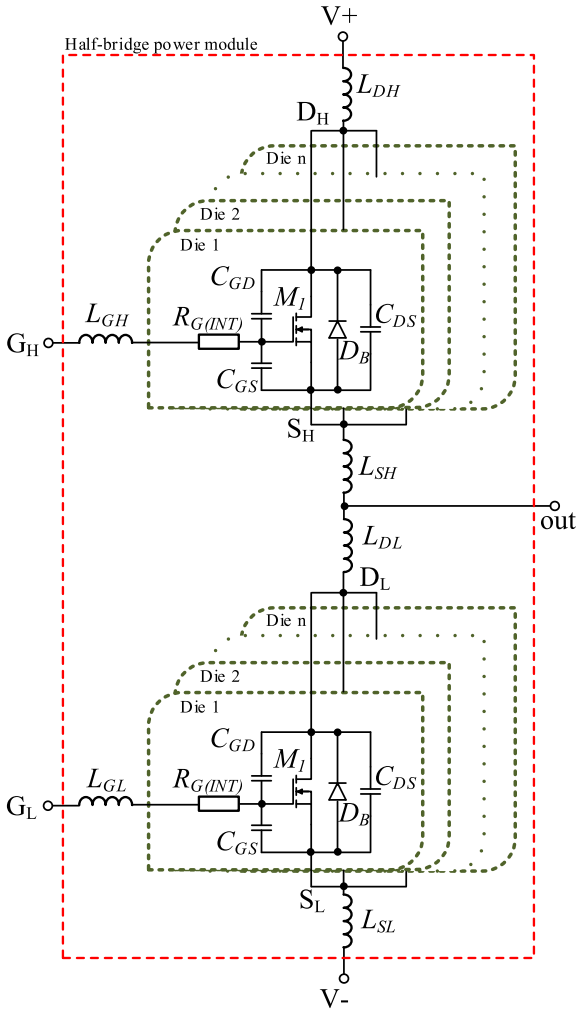

Fig. 2. Simplified equivalent circuit with parasitic capacitances of a multichip SiC MOSFET half-bridge power module.

III. C_{OSS}–V_{DS} Test Method

A. C_{OSS}–V_{DS} Test Method for the Off-State Device

The method proposed by Rabkowski et al. [12] uses a half-bridge power module (scheme in Fig. 3, photograph of the laboratory setup in Fig. 4) similar to [26], but only a single pulse test is performed. The low-side transistor of the half-bridge is the device under test (DUT) and is permanently in the OFF-state, with $V_{GS} < V_{TH}$, while the upper transistor plays the role of the control switch, applying a positive voltage to its gate V_{ctrl} in order to establish a constant voltage V_{DC} to V_{DS} of the DUT. In consequence, the output capacitance of the lower transistor is charged via the upper transistor. There is no resistor in series to limit the current slope, but an increased gate resistor R_G is applied to control the switching speed and peak of the charging current i_{Coss}.

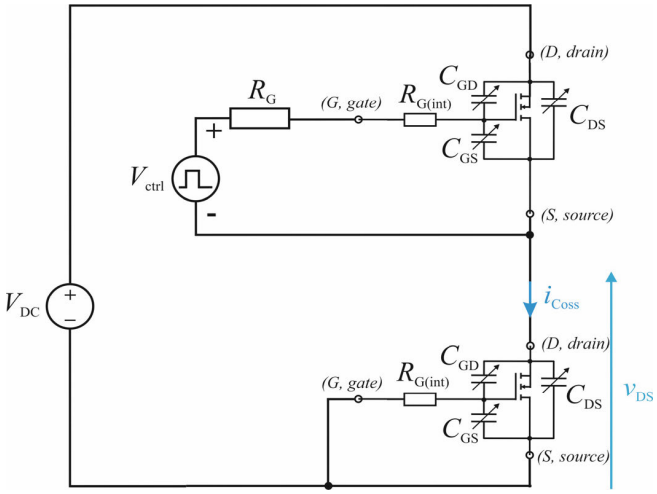

Fig. 3. Half-bridge test setup for the C_{OSS}–V_{DS} characteristic measurements of the SiC power module.

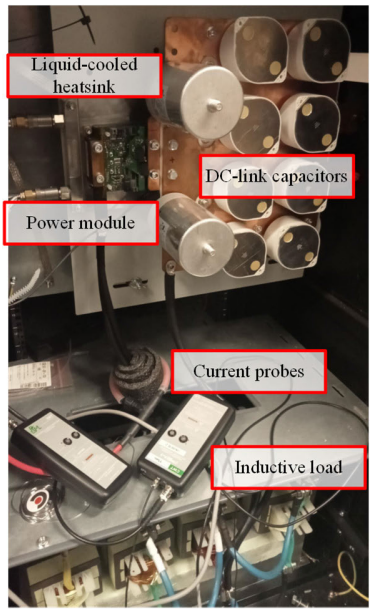

Fig. 4. Photograph of the laboratory setup with the SiC power module used for the experiments.

An example of the waveforms obtained for a 1.7-kV/900-A SiC MOSFET power module, for which C_{OSS}–V_{DS} characteristic is not available in its datasheet, is presented in Fig. 4 for a test performed at 1200-V dc voltage. At the beginning of the process, V_{DS} is low, and the capacitance shows maximum values; therefore, the charging current rises fast and reaches peak value when the V_{DS} slope becomes linear. Then, while the voltage increases, the output capacitance drops, and the charging current is reduced. Note that a similar current also discharges the capacitances of the upper transistor. At the end of the test, the V_{DS} slope becomes nonlinear again, most likely, due to increased capacitance of the upper transistor. All in all, the single pulse takes a few microseconds, and the recorded voltage and current waveforms are employed to perform the

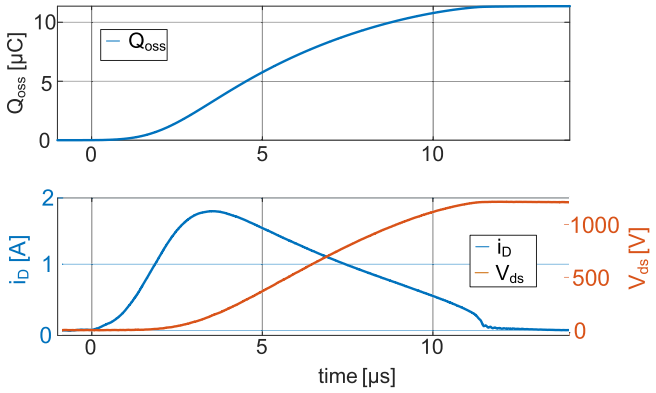

Fig. 5. Waveform of the drain current and drain–source voltage during a test of MSM900FS17ALT power module.

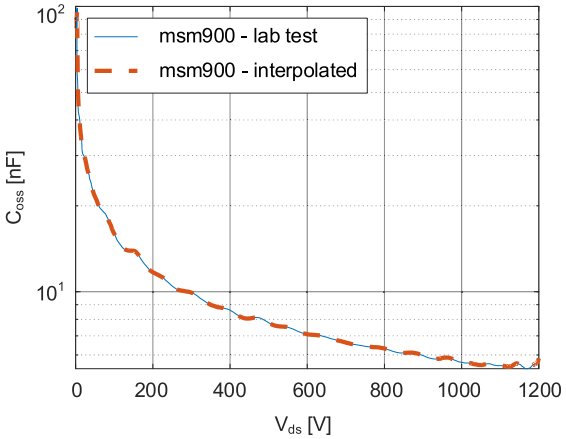

Fig. 6. Measured C_{OSS}–V_{DS} characteristics for MSM900FS17ALT.

calculations according to the basic capacitor formula

$$C_{OSS} = \frac{i_{COSS}}{dV_{DS}/dt}. \tag{1}$$

The calculation of (1) based on the waveforms in Fig. 5 was conducted in MATLAB, and the obtained C_{OSS}–V_{DS} characteristic is shown in Fig. 6. The obtained results have proved to be consistent with those obtained for a 1200-V/450-A SiC MOSFET power module compared to the characteristic available in its datasheet [34].

B. C_{OSS}–V_{DS} Test Method With Nonzero Turn-Off Voltage V_{GS}

As was mentioned above, several works reported the dependence of the capacitances on the turn-off gate-to-source voltage V_{GS-OFF} applied by the gate driver [15], [29], [30]. Therefore, further tests were conducted, with turn-off voltages ranging from −9 to +2 V applied, while the rest of the testing procedure was performed identically to what has been described before. In accordance with the theoretical assumptions, the impact is visible for low V_{DS} values [see Fig. 7(a)], where tests performed at low dc voltage are shown, while for higher V_{DS}, the differences were minimal, and thus, the results at high V_{DS} are not shown. Due to increased C_{GD} at higher V_{GS-OFF}, the C_{OSS} characteristic rises at low V_{DS} voltages,

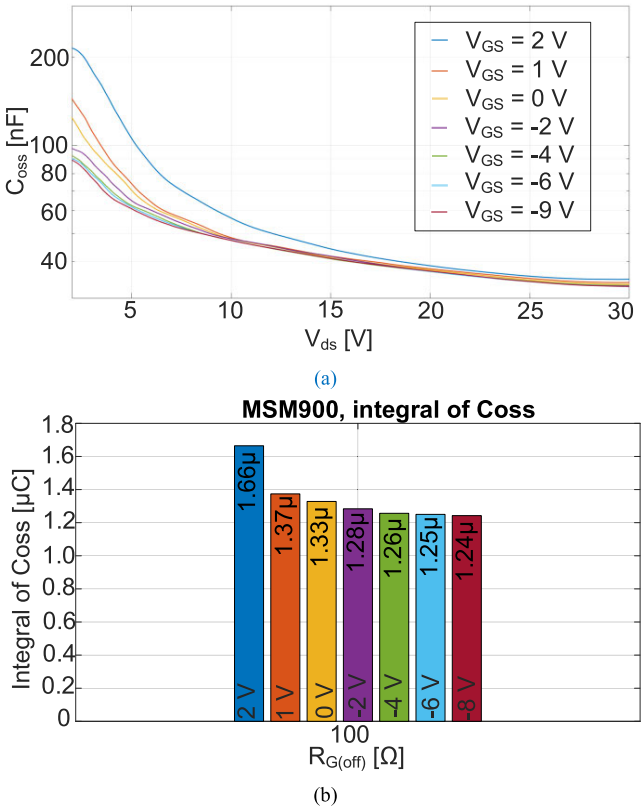

Fig. 7. (a) Dependence of measured C_{OSS} capacitance on the gate–source voltage value for low V_{DS} values. (b) Its impact on C_{OSS} integrated from 0 to 30 V of V_{DS}.

especially when V_{GS} is close to or above zero. In consequence, the charge Q_{OSS}, calculated as (2) for V_{DS} voltages up to 30 V, increases with the increase of V_{GS} [Fig. 7(b)]. The obtained results reflect that turning off at a voltage of −9 V results in a lower Q_{OSS}, meaning a lower switched current is required to achieve ZVS successfully. This difference is below 10% comparing turning off at 0 and −9 V, but the difference can be even as high as 30% comparing +2 and −9 V

$$Q_{OSS} = \int C_{OSS} dV_{DS}. \tag{2}$$

The gate voltage indisputably affects the C_{GD} capacitance, which notably impacts the transistor switching performance. This is caused by the influence of the gate voltage on the drain depletion layer beneath the gate oxide capacitance, which is dependent on the $V_{GD} = V_{GS} - V_{DS}$. However, the whole MOSFET output capacitance C_{OSS} required for estimating the channel current from V_{DS} value is dominated by the C_{DS} part, which is mainly unaffected by the change in gate–source voltage. Furthermore, the most notable shifts in capacitance occur for low drain–source voltages when the dissipated losses are rather low. When the switching turn-off power losses are considered, the crucial is the area for roughly 20%–80% V_{DS}, where the current is still on a significant level, while the voltage already reaches notable values, and the product (power loss) is eminent. Thus, the overall impact of the V_{GS} level on the proposed method can be easily neglected as the slight variations most likely still appearing in the C_{GD} component

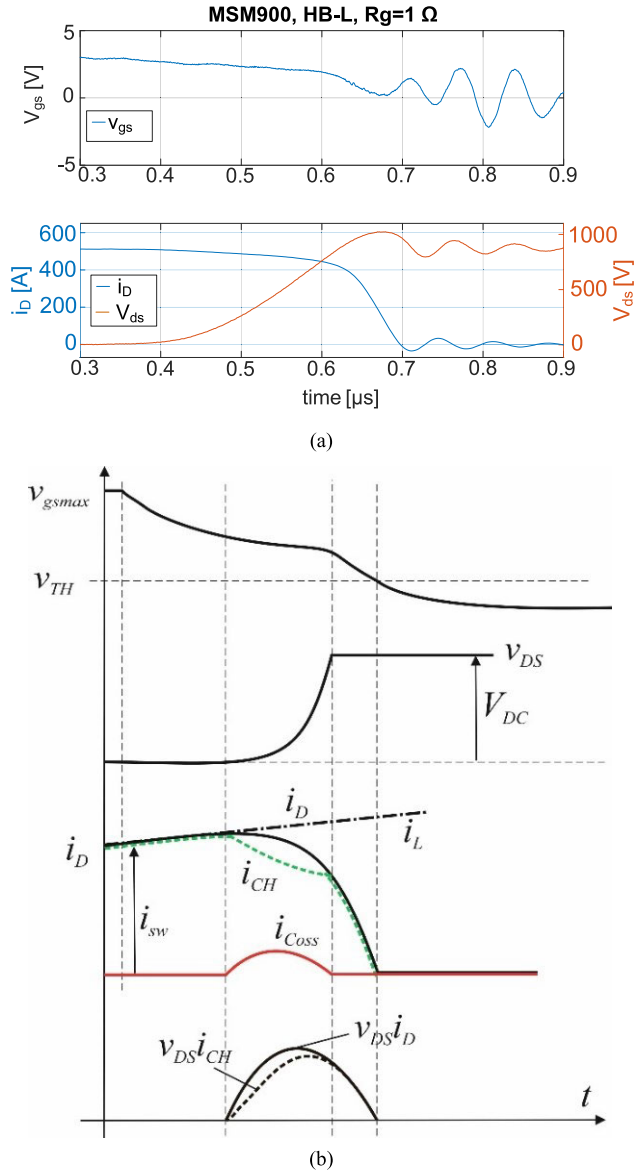

Fig. 8. (a) Waveforms during turn-off—recorded for the MSM900FS17ALT. (b) Idealized—without an influence of the parasitic inductance.

are so minuscule that are not distinguishable among the discrepancies and accuracy of the measurements. All in all, based on the performed tests and according to the MOSFET structure, the C_{OSS} capacitance is effectively independent of the gate polarization value, at least in terms of C_{OSS}–V_{DS} characterization for channel current estimation.

IV. Difference Between Drain and Channel Currents

Several typical waveforms recorded at the turn-off process of the MSM900FS17ALT at 850 V and 600 A are presented in Fig. 8(a), while idealized equivalents can be seen in Fig. 8(b). To simplify, the impact of parasitic inductances and high-frequency oscillations is not considered. In the optimal scenario from the switching losses point of view, the gate driver can quickly discharge the gate–source capacitance C_{GS}

to reach threshold voltage V_{TH} before drain–gate capacitance C_{GD} is charged and drain–source voltage v_{DS} achieves high values. The current through the channel of the power transistor i_{CH} is rapidly reduced to zero before v_{DS} is high, and, as a result, the power dissipated in the transistor (as the product of v_{DS} and i_{CH}) is low. These conditions can be recognized as almost ZVS, and this scenario is preferable as it results in nearly zero switch-on losses and therefore leads to higher efficiencies [7].

However, this scenario is challenging to achieve in most high-current power modules. The substantial input capacitance C_{ISS} requires a large gate current to be quickly discharged, but the limited supply voltage of the gate driver and nonzero internal gate resistance are the limiting factors. Thus, the real scenario usually observed is presented in the idealized waveforms in Fig. 8(b): during the voltage rising phase, the v_{GS} is above the threshold, and the channel remains open. This causes a major difference in the estimation of the switching power losses since the only source of power losses is the joule losses caused by the channel current through the device resistances, while the displacement current charging the output capacitance is not contributing to these power losses. Therefore, the resulting power losses are lower than the product of v_{DS} and i_D multiplication usually provided in the datasheets. Finally, v_{GS} drops below V_{TH} (and i_{CH} becomes zero) after v_{DS} has reached V_{DC}. It is worth noting that, at the end of the voltage rise phase, the observed i_D is equal to i_{CH}, since there is no displacement current in the output capacitances C_{OSS} when the voltage has reached a constant value. In practice, it will also be increased by voltage overshoots across parasitic inductances in the switching loop, as shown in Fig. 8(a).

V. Estimation of I_{COSS} and I_{CH}

The MSM900FS17ALT has been arranged in a half-bridge circuit supplied from an 850-V source and loaded with an inductive load (3 × 114 μH/100 A in parallel) with negligible resistance, so that the power circulates between the two power switches. The scheme of the experimental test system is presented in Fig. 9, using the same experimental setup as before but with an inductive load (shown in Fig. 4). Then, the transistors were controlled to generate a square voltage wave in the load to obtain a different amplitude of the load current, with a variable switching frequency up to 25 kHz, which is a typical value for high-power semiconductor modules as used in the article. These conditions lead to a triangle shape of the load current and switching conditions similar to those in soft-switched dc–dc converters. In particular, the transistors turn on with the current flowing through the antiparallel diode, and therefore, the on-state voltage is close to zero and turns off at peak load current. Thus, most of the power losses appear during the turn-off event twice per single switching period. In the circuit in Fig. 9, the drain–source voltage and drain current waveforms were measured with the high-bandwidth voltage probe (P5200A) and Rogowski coil. Examples of the results from the experimental study for different switched currents, along with the estimations of the channel and capacitive currents are depicted In Fig. 10 and Fig. 11 for

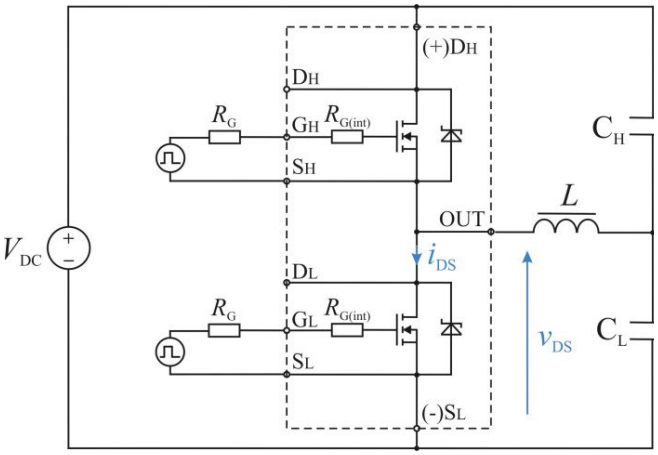

Fig. 9. Scheme of the half-bridge circuit with an inductive load.

$R_{G(EXT)} = 3.3\ \Omega$, and in Fig. 12 and Fig. 13 for a case without an external gate resistor. The switching process is faster for the higher current and lower gate resistance; the same observation can be made for the oscillations—they become more severe for the higher current and lower gate resistance.

The C_{OSS}–V_{DS} characteristic determined at $V_{GS\_OFF} = 0$ V before (Fig. 6) has been employed to calculate the capacitive current i_{COSS} during the switching process as (3), calculating the derivative of the drain–source voltage dv_{DS}/dt in MATLAB based on the measured waveforms

$$i_{COSS} = C_{OSS}(v_{DS})\frac{dv_{DS}}{dt}. \tag{3}$$

Furthermore, in order to take into account the voltage drop in the stray inductance inside the power module and therefore obtain more accurate results, v_{DS} in (2) was replaced by the internal $v_{DS(i)}$ calculated as

$$v_{DS(i)} = v_{DS} - L_S\frac{di_D}{dt} \tag{4}$$

where L_S is half of the internal module inductance provided by the datasheet. The obtained results are presented in Figs. 11 and 13 for $R_{G(EXT)} = 3.3\ \Omega$ and without an external gate resistor, respectively.

As can be observed based on Figs. 11 and 13, the effect of the capacitor current on the power loss estimation is substantial. For the low current operation of the power module (100-A switched current), the resulting relative error of the switched energy because of capacitor current omission can be as high as 100%, while for a high current test (600 A), it reaches slightly above 7%. However, considering a system at several hundred kilowatts, or single megawatts of power, this is still a substantial value in terms of the thermal design of the system, and thus, the effects of C_{OSS} and its' current should not be omitted, and the suggested C_{OSS}–V_{DS} characteristic obtaining method can be an invaluable tool for improving the design of high-power converters.

VI. Discussion

A closer analysis of the i_{COSS} waveforms presented in Figs. 10 and 12 shows that they are almost independent of the switched drain current. Only at the lowest currents, the

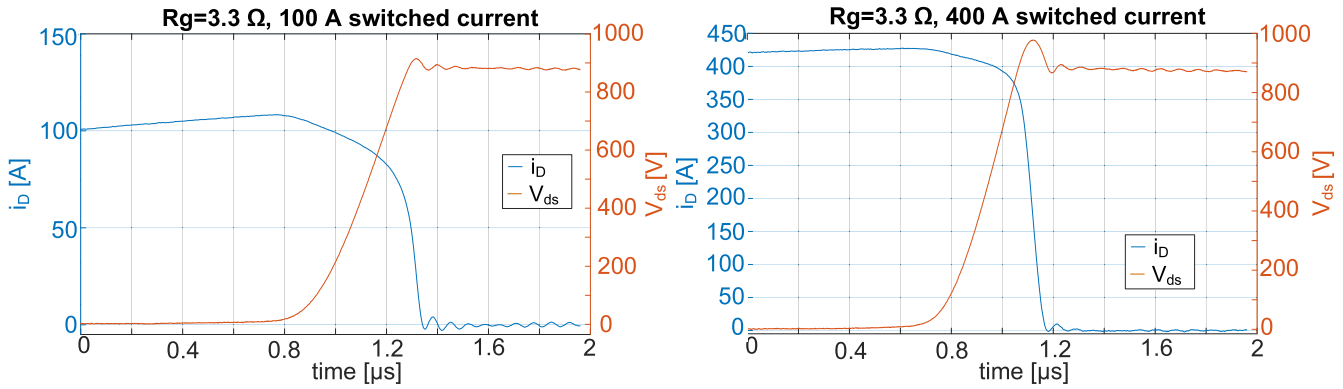

Fig. 10. Turn-off process for $R_{G(EXT)} = 3.3\ \Omega$ at 850 V and (a) 100 and (b) 400 A, measured values.

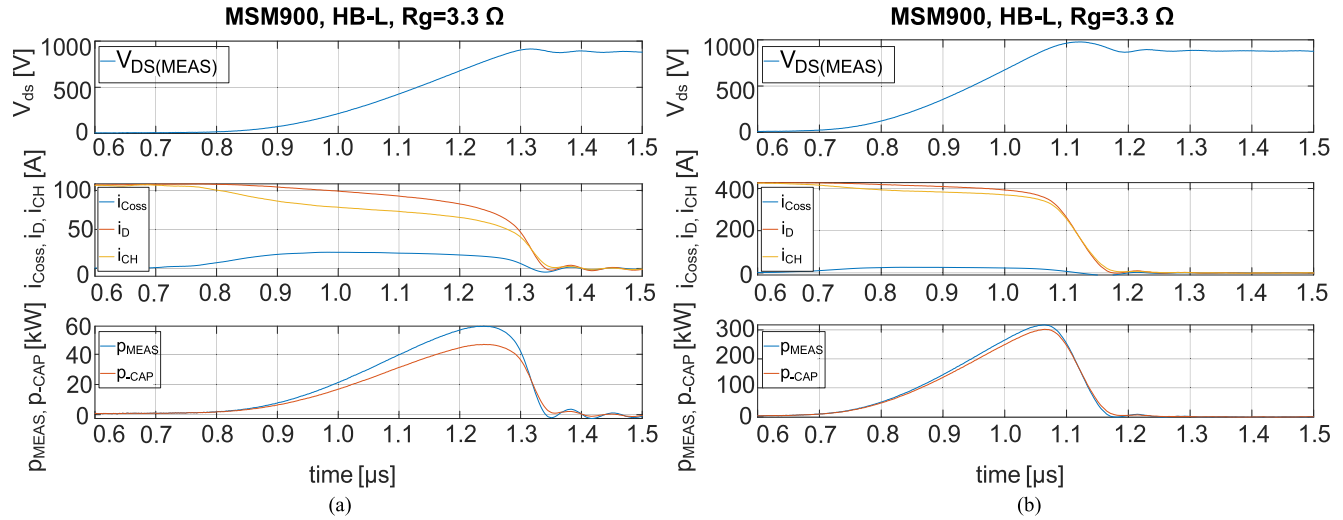

Fig. 11. Estimation of i_{COSS} and i_{CH} and resulting power losses for $R_{G(EXT)} = 3.3\ \Omega$ at 850 V and (a) 100 and (b) 400 A.

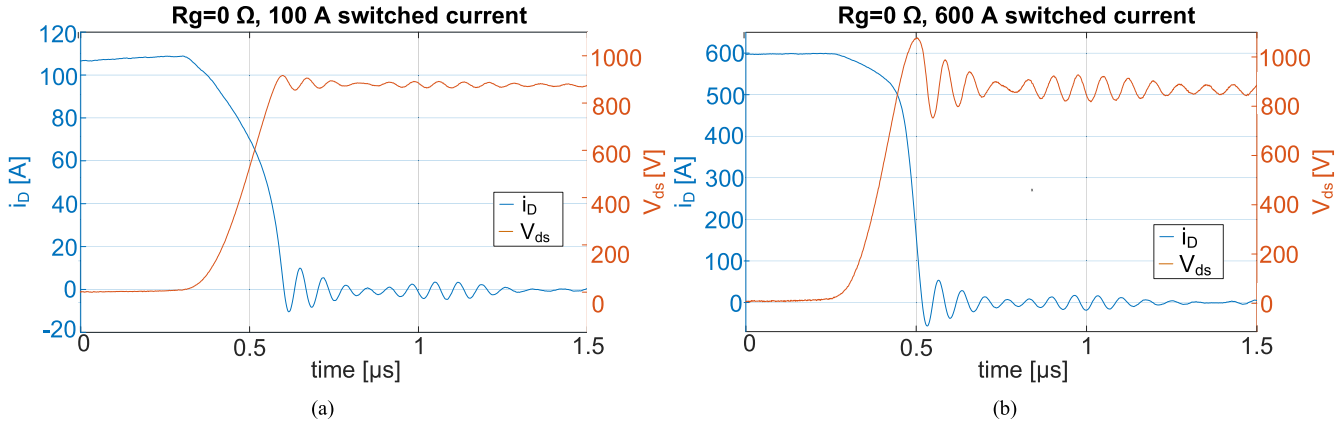

Fig. 12. Turn-off process for $R_{G(EXT)} = 0\ \Omega$ at 850 V and (a) 100 and (b) 600 A, measured values.

resulting i_{COSS} has presented differences, since the lack of switched current resulted in a longer voltage rising and a lower peak i_{COSS}. The major impact on the shape of i_{COSS} is the decrease of the gate resistance, resulting in a much higher switching speed. In particular, the peak value of the i_{COSS} is higher for faster switching. Both observations indicate that i_{COSS} is mainly the result of the charge displacement related to the changes in the drain potential. For the cases shown in Figs. 10 and 12 but also for two more gate resistance values [$R_{G(EXT)} = 1.6$ and 1 Ω], the waveforms of i_{COSS} were integrated to determine the charge Q_{OSS} (see results in Fig. 14). The values should be constant but vary between 8.9 and 9.7 μC (~9% of the total error), which may be considered an acceptable value resulting from the measurement

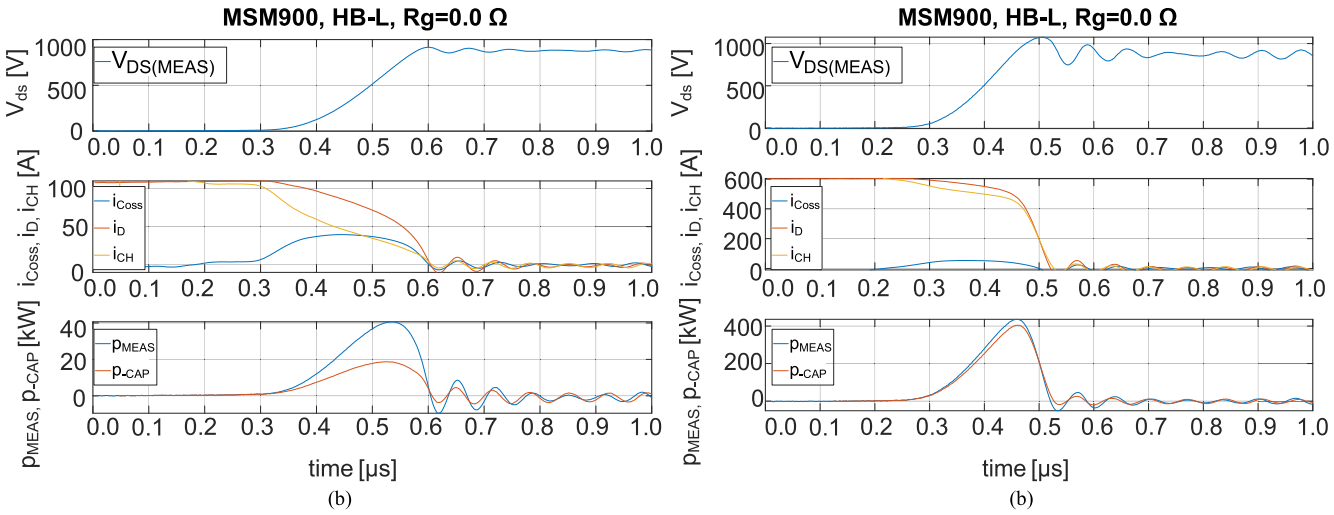

Fig. 13. Estimation of i_{COSS} and i_{CH} and resulting power losses for $R_{G(EXT)} = 0\ \Omega$ at 850 V and (a) 100 and (b) 600 A.

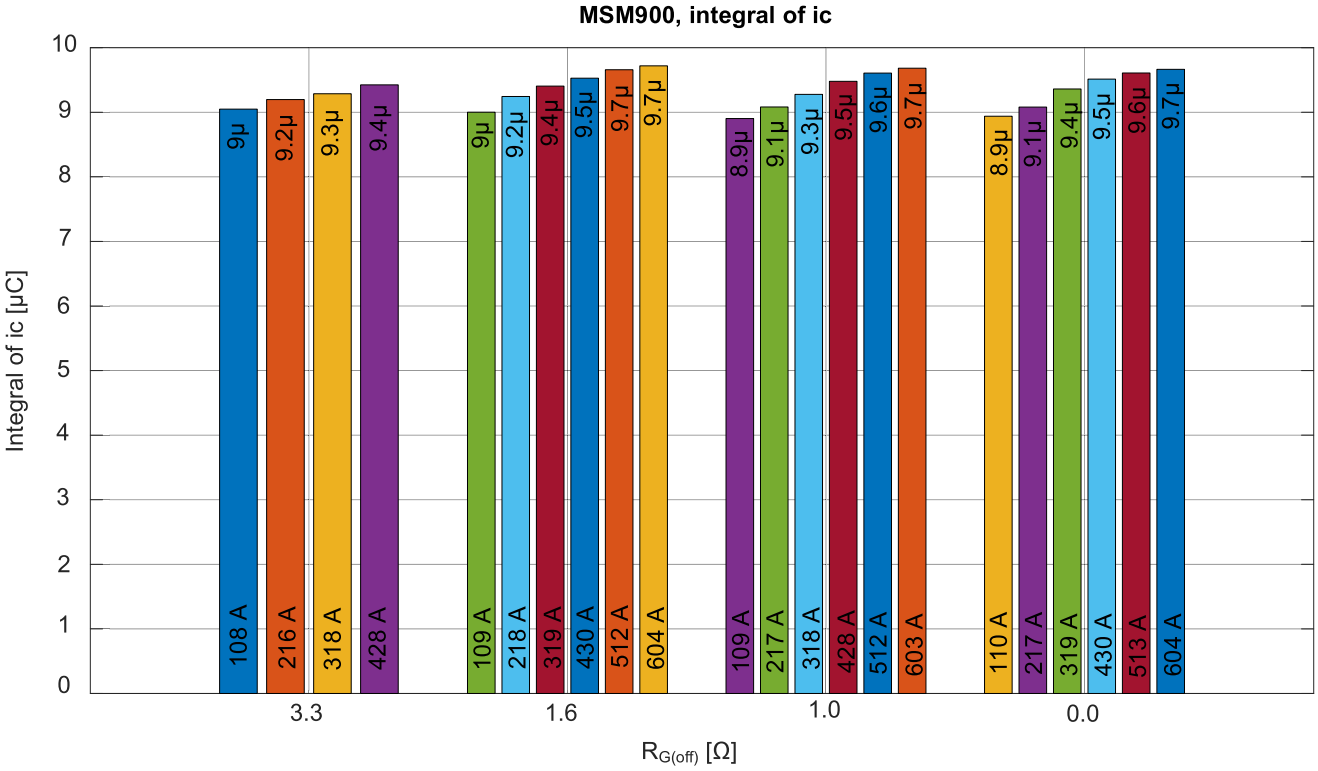

Fig. 14. Calculated Q_{OSS} at 850 V and different gate resistances and switched currents.

discrepancies. They rise with the switched current for all cases, which is, most likely, a result of higher voltage overshoot (increasing with the switched current and decreasing with the gate resistance). Note that the values for the same switched currents show minimal differences; thus, the obtained error from the measurements is in the half-bridge circuit rather than in the obtained $C_{OSS} - V_{DS}$ characteristic.

VII. Conclusion

This article presents a novel method for obtaining the $C_{OSS} - V_{DS}$ characteristics for SiC power modules. Its main advantage is a simple application within the half-bridge module without additional effort—a low-power, high-voltage power supply and typical voltage and current probes are necessary. The setup is very similar to the one required for double-pulse tests and power loss characterization of power devices. The test for the 1.2-kV/425-A module has shown very good agreement with the $C_{OSS} - V_{DS}$ characteristic provided by the manufacturer, and the method was also applied to the 1.7-kV/900-A module, for which the datasheet is unavailable.

Based on the measured characteristic, the capacitive current i_{COSS} has been calculated for this same module operating in the continuous mode at 850 V at different switching speeds with currents up to 600 A and switching frequencies up to

25 kHz. Then, Q_{OSS} was determined for all cases. Under the assumption that Q_{OSS} should be constant for all tested cases, the authors have determined errors in the whole procedure at the level of ±4.5%. It is very likely that most of the error comes from the different voltage overshoots across the parasitic inductances. All in all, for the fast-switching SiC power devices, this is an acceptable value to increase the accuracy of power losses estimation of soft-switched dc–dc converters that can help to improve the design process of highly performant, high-power power electronic systems in medium voltage range.

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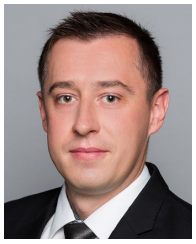

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3.2 A Simple Method to Validate Power Loss in Medium Voltage SiC MOSFETs and Schottky Diodes Operating in a Three-Phase Inverter [P2]

[P2] J. Rąbkowski, H. Skoneczny, **R. Kopacz**, P. Trochimiuk, G. Wrona, "A Simple Method to Validate Power Loss in Medium Voltage SiC MOSFETs and Schottky Diodes Operating in a Three-Phase Inverter", Energies, 13, 4773, 2020. Points according to the Ministry of Education and Science: **140**, Impact Factor: **3.252**. Contribution of the dissertation author: **25%**. [131]

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A Simple Method to Validate Power Loss in Medium Voltage SiC MOSFETs and Schottky Diodes Operating in a Three-Phase Inverter

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Abstract: This paper presents an original method of power loss validation in medium-voltage SiC MOSFET (metal–oxide–semiconductor field-effect transistor) modules of a three-phase inverter. The base of this method is a correct description of the on-state performance of the diodes and the transistors in a PWM (pulse width modulation)-controlled inverter phase leg. Combined electro-thermal calculations are applied to precisely estimate the losses in the power devices and then, to find the suitable circuit parameters of a test circuit to emulate these conditions. A simple square-wave-controlled half-bridge with an inductive load enables the electrical and thermal stresses comparable to these in the inverter, and moreover, provided equations that confirmed the possibility of balancing the load between the diodes and the transistors. The circuit with 3.3 kV SiC MOSFETs was tested to verify the impact of selected parameters on power losses with the main focus on duty ratio. The same module was applied, in addition to an inductive load (3 × 112 µH) and two sets of DC-link capacitors (750 µF), to validate a phase leg of a 220 kVA inverter. In spite of a significantly apparent power, the active power delivered from the DC supply settled around 1 kW, which was enough to emulate 390 W of losses in two transistors and diodes.

Keywords: medium voltage; inverter; SiC MOSFET; Schottky diodes; power losses

1. Introduction

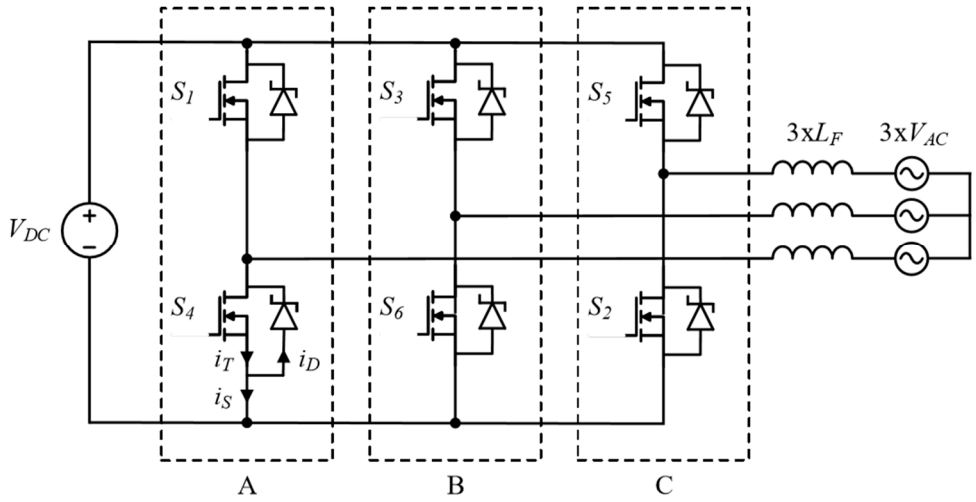
Nowadays, research works on medium-voltage power conversion with silicon carbide (SiC) power devices can be divided into two substantial parts. The major interest of researchers seems to be focused on relatively new devices rated at 10 kV and more [1–3], mostly developed for power grid applications, where direct silicon (Si) competitors do not exist due to physical limits. On the other hand, recent literature reports also show 3.3 kV rated power modules with SiC MOSFET (metal–oxide–semiconductor field-effect transistor) and Schottky diodes, competing against well-established Si IGBTs (insulated gate bipolar transistors), usually in motor drive inverters [4,5]. The major advantage is the much faster switching of SiC unipolar devices, cutting down the amount of energy dissipated during turn-on and turn-off processes [6]. However, a comparison of the on-state performance is not that conclusive as IGBTs show a lower voltage drop at higher current ratings while SiC MOSFETs show the ability to conduct reverse currents. This issue has been already investigated in the literature, to mention only [7–12], where the performance of SiC FETs in the inverter phase leg was studied. A typical inverter leg with a standard switch based on Si IGBT requires the forward diode to carry the reverse current, while in the MOSFET–Schottky pair, the majority of this current flows through

low-resistive substrate and channel. This means that the antiparallel SiC Schottky is mostly utilized during dead-time periods. Therefore, most of the existing knowledge regarding the transistor and diode pair operating inside the power module of the inverter is obsolete for SiC devices. On the base of the experiences of the authors of this paper, datasheet information describing on-state and dynamic performance show limited value in a complex electro-thermal process of medium-voltage power converter design. Moreover, a well-known double pulse test procedure can be used to verify the switching performance, however, the outcomes may vary in the final system due to the different distribution of parasitic capacitances and inductances [13]. Thus, new challenges in the design process of power converters based on medium-voltage SiC power devices generates the need to research new methods which enable continuous operation testing, without building an expensive fully scaled inverter. The main requirement is simplicity, which will be always related to low cost as all complex methods in medium voltage and high-power range require expensive set-up and equipment. The ability to accurately measure the power loss is essential as well. Previous experiences show that problems related to the measurement and the estimation of losses in power electronic converters have always been as challenging as important [14,15]. The right measurement of power losses is even harder for wide band-gap power devices, especially when higher electromagnetic interferences occur and the amount of measured losses is low. Unfortunately, the most obvious method based on input and output power measurement would require extremely precise current and voltage measurements [16], which, for medium voltage, is extremally difficult and also expensive. A number of calorimetric methods [16–20] enable the measurement of overall efficiency, however, dividing the power losses between passive and active elements requires additional effort, which again, for medium-voltage conditions, is challenging. Moreover, the design of the calorimetric setup for medium-voltage converters characterized by high volume is also problematic, especially when isolation requirements are taken into account. As mentioned above, electrical-based measurements may bring accurate results by double-pulse measurements [21,22] with an additional focus on measurement techniques [23], however, in the final converter the performance of the devices may differ. This issue is even more visible for medium-voltage devices as the layout of the double-pulse setup is hard to repeat in the converter, which leads to differences in the parasitic components influencing the switching behavior. In response to this issue, several methods that reflect the real conditions in power converter systems have been proposed. Most common are those derived from opposition methods [24] and use a full-bridge topology [25–29]. However, the design of such a system with two half-bridge modules almost equals the design of a three-phase inverter, which means complexity and high expenses. Other solutions based on DC–DC [30,31] or half-bridges can be also found [32] in the literature but they were, again, proposed for low-power SiC or GaN devices and are not suitable for medium-voltage/high-power systems, where the main problem is the power dissipation. Even for the resistive load power at a fraction of the high rated power of a medium-voltage converter, this ends in tens of kWs to dissipate in laboratory conditions.

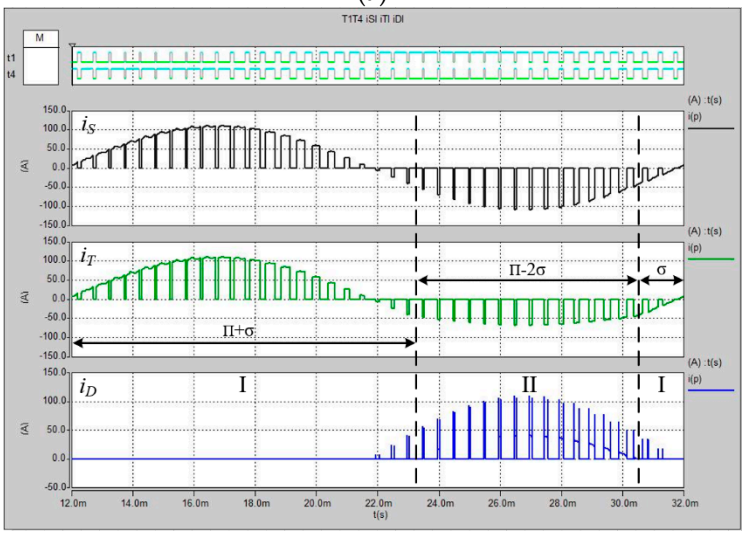
All these works were carefully studied to find a suitable solution for a very challenging process of medium-voltage SiC inverters design and testing. As a consequence, a novel method using simple measurements in the half-bridge circuit and precise electro-thermal calculations is proposed to emulate the power losses of the module applied in a three-phase inverter. This method and their experimental validation can be counted as a main contribution of this paper. In particular, the precise equations describing on-state losses in the three-phase inverter including reverse conduction phenomenon and dead-times is provided in Section 2. Moreover, the behavior of the half-bridge with the inductive load is explained and described for the first time to provide background for precise power loss emulation in SiC MOSFETs and Schottky diodes. Section 4 presents the experimental validation of the equations presented in Section 2, by the means of power loss measurements for various voltages, switching frequencies and duty ratios, which is also an original content of this paper. Finally, a showcase of the proposed method by means of power loss estimation and validation for selected the operating point of a three-phase inverter is shown in Section 5, while Section 6 concludes the paper.

2. Power Module with SiC MOSFETs and Schottky Diodes in a Three-Phase Inverter

In contrast to low-voltage applications, medium-voltage SiC power devices operate only inside isolated power modules [1,3–6]—usually in half-bridge configuration [33–35]. Such a module can be a part of an isolated or non-isolated DC–DC converter, however, the most common application is a three-phase inverter composed of three pieces—see Figure 1a. For the sake of simplicity, let us consider a general case when the inverter is supplied from DC voltage source V_{DC} and connected to three-phase inductive load ($3 \times L_F$) also including three-phase AC voltage sources ($3 \times V_{AC}$). Energy may be transferred in both directions and the power factor may vary between −1 (rectifier mode) and 1 (inverter mode) by means of AC current control. However, while the more complex control issues are out of the scope of this paper, due to the focus on the methods' simplicity, a straightforward carrier-based sinusoidal PWM (pulse width modulation) method was assumed and expected to result in balanced AC currents at three-phase outputs. Under such circumstances, all six switches operate under identical conditions by means of switching and conduction losses and thus only one—the lower switch from phase A (S_4 in Figure 1a)—is the subject of further consideration. To illustrate the performance the control signals and waveforms of currents in the switch (i_S), the transistor (i_T) and the diode (i_D) are presented in Figure 1b for a power factor near unity.

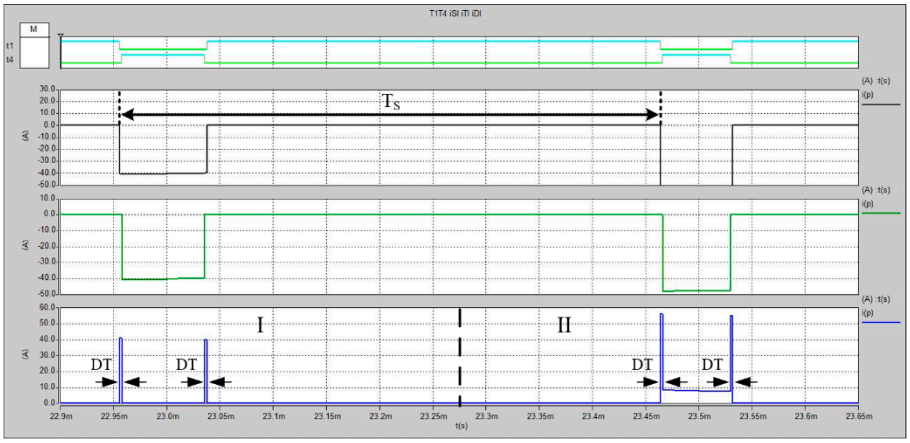


(**a**)



(**b**)

Figure 1. *Cont.*



(**c**)

Figure 1. Three-phase inverter (**a**), typical waveforms of the MOSFET (metal–oxide–semiconductor field-effect transistor) and diode currents over one fundamental period (**b**) and the same waveforms illustrating a border between the first and second phase (**c**).

2.1. Switching Losses

A well-known feature of the inverter phase leg controlled with a sinusoidal PWM method is that two switching transitions occur during period T_S and the phase current always commutates within a transistor–diode pair. Therefore, after an assumption that current ripples can be neglected and the amplitude of phase currents equals to I_M, switching losses of single transistor P_{SWT} and diode P_{SWD} operating in an inverter leg, according to the well-known relationship [36], can be described as

$$P_{SWT} = \frac{f_s V_{DC} I_M}{\pi V_T I_T}(E_{on} + E_{off}), \tag{1}$$

$$P_{SWD} = \frac{f_s V_{DC} I_M E_{REC}}{\pi V_T I_T}, \tag{2}$$

where f_s is the switching frequency, E_{on} and E_{off} are the energies dissipated in the transistor during the turning on and turn off processes obtained for voltage V_T and current I_T, while E_{REC} is the diode switching energy. Please note that this equation assumes a linear dependence of switching energies, which for SiC MOSFETs is usually considered true.

2.2. On-State Performance

In terms of on-state performance, the SiC MOSFET/Schottky pair can be recognized as more complex than the most common solution in medium-voltage inverters which is a pair of an Si IGBT and a forward diode [7–13]. A closer look at the waveforms in Figure 1b shows that, in addition to conducting the current during short dead-time periods, the diodes also share a negative current of the switch with MOSFETs at some specific circuit conditions. Thus, the transistor takes the whole switch current not only during the positive sign of i_S, but also in areas defined in Figure 1b by angle σ as well. The reason for such behavior is the existence of the voltage of the built-in Schottky contact V_{TO} (relatively high in SiC, usually slightly below 1 V) and the very low on-state voltage drop $V_{SD(ON)}$ across the resistances of MOSFETs counted in single milliohms. When $V_{SD(ON)} < V_{TO,}$ the diode is turned-off after a dead-time period under zero voltage conditions—this case can be seen in the left switching period in Figure 1c. In the next switching period, the reverse current is higher, $V_{SD(ON)} > V_{TO}$

and the diode conducts in parallel to the MOSFET. As presented in [10] the angle σ is related to the phase current and parameters of the devices, specifically, and it may be described as

$$\sigma = \arcsin\frac{V_{T0}}{r_{ON}I_M}, \tag{3}$$

where r_{ON} is the on-resistance of the conducting SiC MOSFET. As a consequence, two basic areas may be distinguished as in Figure 1b:

- Area I when only the transistor is conducting (excluding dead-time periods), duration ($\pi + 2\sigma$);
- Area II when the transistor and diode share a negative current ($\pi - 2\sigma$).

Previously, the impact of the dead time on the on-state losses was neglected in the author's works [10,37,38], however, in some operating points, it may be noticeable. Therefore, a "dead-time duty factor" γ is introduced as

$$\gamma = \frac{T_{DT}}{T_s}, \tag{4}$$

where T_{DT} is the single period of dead time (occurs two times per switching period). Using the same approach as in [10], the transistor on-state power loss for the area I can be described as

$$P_{CT}{}^{I} = \frac{r_{ON}I_M^2}{4\pi}\left(\frac{\pi}{2} + \sigma - \gamma(\pi + 2\sigma) + sin\,\sigma\,cos\,\sigma(2\gamma - 1) + \frac{m\,cos\,\phi}{6}(9\,cos\,\sigma - cos\,\sigma)\right), \tag{5}$$

where m is the modulation index and ϕ is the phase angle between the phase voltage and current. The remaining part of the loss in the transistor is expressed as

$$P_{CT}{}^{II} = \frac{r_{ON}}{4\pi\sum_{r^2}}\left[\begin{array}{c} V_{TO}{}^2((1-2\gamma)(\pi-2\sigma) - 2m\,cos\,\phi\,cos\,\sigma) \\ + r_D V_{TO} I_M(4\,cos\,\sigma\,(1-2\gamma) + m\,cos\,\phi\,(2\sigma - \pi - sin(2\sigma))) \\ + \frac{r_D{}^2 I_M{}^2}{2}\Big((1-2\gamma)\Big(\pi - 2\sigma\Big) + (1-2\gamma)sin(2\sigma) + \frac{m\,cos\,\phi}{3}(cos\,3\,\sigma - 9\,cos\,\sigma)\Big) \end{array}\right], \tag{6}$$

where r_D is the series resistance of the diode, Σr is the sum of r_{ON} and r_D and V_{TO} is the threshold voltage of the diode. Similarly, the diode on-state loss during the II area can be expressed as

$$P_{CT}{}^{II} = \frac{r_{ON}}{4\pi\sum_{r^2}}\left\{\begin{array}{c} V_{TO}{}^2(2m\,cos\,\phi\,cos\,\sigma + (2\gamma - 1)(\pi - 2\sigma)) \\ - \frac{(r_{ON} - r_D)V_{TO}I_M m}{2}\Big(cos\,\phi\left(sin(2\sigma) + \pi - 2\sigma\right) + \frac{4cos\sigma(2\gamma-1)}{m}\Big) \\ + \frac{r_{ON}r_D I_M{}^2 m}{6}\Big(cos\,\phi\Big(cos(3\sigma) - 9cos\sigma\Big) - \frac{3}{m}(2\gamma-1)(sin(2\sigma) + \pi - 2\sigma)\Big) \end{array}\right], \tag{7}$$

Additional diode conduction losses during dead time are equal to [12]:

$$P_{CD}{}^{DT} = \gamma\left(\frac{2V_{TO}I_M}{\pi} + \frac{r_D I_M{}^2}{2}\right), \tag{8}$$

In general, the equations presented above prove that the distribution of the current among devices in the MOSFET–Schottky pair of the power module depend on circuit conditions (voltage, currents and power factor), control parameters (modulation index and dead-time duration), as well as temperature-influenced parameters of the devices.

2.3. Power Loss and Junction Temperatures Estimations

The equations presented above along with well-known thermal relationships may be applied to calculate power losses and junction temperatures of the transistors and diodes operating in a three-phase inverter. It is noteworthy that both losses and temperatures are averaged over one fundamental period of the phase current. Temperature variations, which occur in shorter time periods, will not be considered under the assumption that the thermal capacitances of medium-voltage modules and

their cooling system are significant. Another simplification is an assumption of the same temperature of the common heatsink. All in all, the electrical (power loss) and thermal (temperatures) equations may be coupled in one procedure executed until the system reaches steady-state. The diagram of the procedure described more thoroughly in [10,37] is shown in Figure 2. The base for the calculations is a reference between the electrical parameters of the module and the junction temperatures described based on the datasheet and/or previously performed measurements. In the next step, the conduction (P_C) and switching losses (P_S) for the diodes and transistors at room temperature are determined using Equations (1)–(8) and also parameters of the three-phase inverter (phase current I_M, DC-link voltage V_{DC}, power factor $cos\sigma$, switching frequency f_S, modulation index m). Then, the average junction temperatures are calculated on the basis of the thermal parameters of the module and the applied heatsink (R_{THSA}). The next step is to check if the system is in steady state, in particular if the rise of the junction temperatures is lower than the assumed threshold. A negative answer leads to another iteration: electrical parameters are updated according to new junction temperature values and calculations of losses and temperatures are repeated. A positive answer leads to the final results—the steady state junction temperatures of diodes and transistors for given circuit conditions.

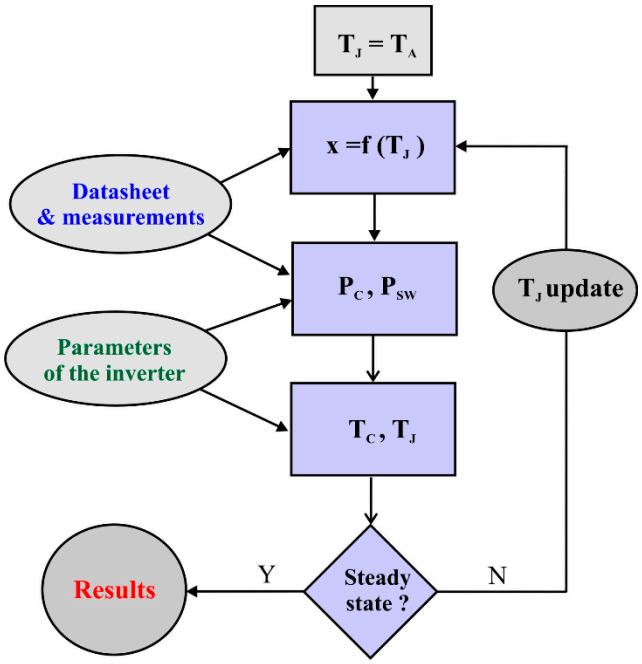
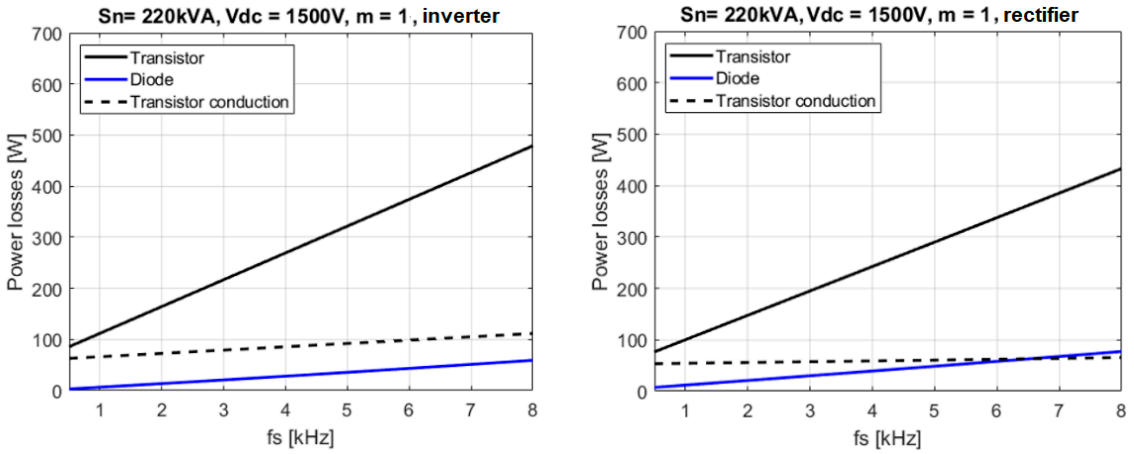


Figure 2. The diagram of the applied procedure to estimate power losses and junction temperatures.

The described procedure was applied to estimate power losses and junction temperatures in transistors and diodes of a three-phase inverter rated at 220 kVA operating at a DC voltage of 1500 V according to the scheme shown in Figure 1a. Each phase leg is assumed to contain a 3.3 kV/450 A SiC MOSFET module from Hitachi MSM450FS33A [38], and all three modules are mounted on a common liquid-cooled heatsink (R_{THSA} = 15 K/kW). Switching energy values were determined on the basis of double-pulse test measurements using an in-house gate driver [38]. The calculations were performed for variable switching frequency and two different power factor values—see Figure 3. As expected, the power losses rise with the switching frequency, and slightly higher values are also observed for the unity power factor in the inverter mode (see in Figure 3a) as during the rectifier mode (see Figure 3b), diodes and transistors share more reverse current.



(**a**) (**b**)

Figure 3. Power losses vs. switching frequency for inverter mode (**a**) and rectifier mode (**b**)—an estimation for a 220 kVA inverter.

3. Power Losses Validation in a Half-Bridge Circuit

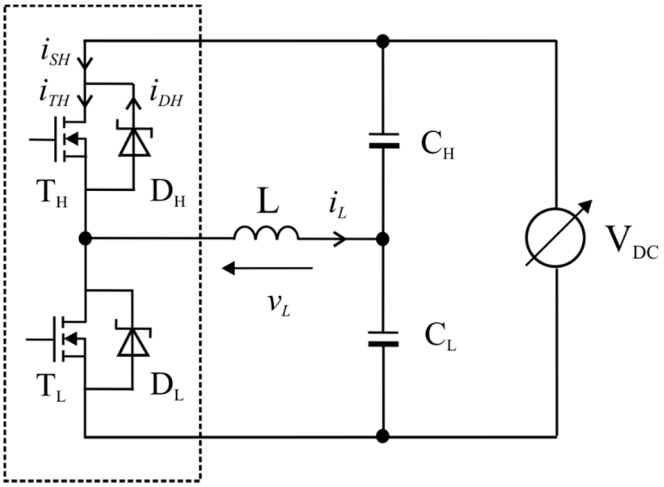
The method of estimating the electrical and thermal behavior of the transistors and diodes presented in the previous section is strongly influenced by the accuracy of applied data. In practice, with lower precision, a risk of the thermal runaway is increased, or, on the other hand, higher safety margins may lead to oversizing the cooling system. Obviously, the accuracy of the estimations can be elevated by the use of the double-pulse tests and measurements with curve tracers by means of more real data. However, the best verification would be a design of a full three-phase inverter or validating at least a single phase leg. It is worth noting that for the medium-voltage SiC-based systems, this is accompanied by high costs, complicated measurements, and therefore, simple methods of the electrical and thermal validation may be a better option. Therefore, a novel method using a half-bridge circuit with an inductive load is proposed to meet the expectations of medium-voltage inverters. The main idea is to reproduce the electrical and thermal conditions of the power module operating in a three-phase inverter using a simpler circuit—the square-wave controlled half-bridge with an inductive load.

The circuit (Figure 4a) and layout are similar to a single-phase of an inverter, and electrical and thermal features close to the final design can be achieved. The required amount of active power from a DC supply is limited as energy is circulating between capacitors C_H/C_L and load inductor L. The method is very simple—the operating conditions can be adjusted by means of the supply voltage V_{DC}, the inductance L and the switching frequency f_{SH}. Moreover, changes of the transistor duty ratio D decide on the precise distribution of the power losses between the transistors and diodes to precisely reproduce the conditions in a three-phase inverter, also including the reverse conduction of SiC MOSFETs. As will be presented in next sections, power loss measurements are not complex and the level of electromagnetic interferences is lower than in the inverter due to soft-switching between transistors and diodes. Finally, due to just a few necessary components (single half-bridge module, inductor, two sets of DC capacitors), also in terms of measurement equipment (power meter, cooling system), and simple open-loop control without sensors, the method can be recognized as relatively low in cost.

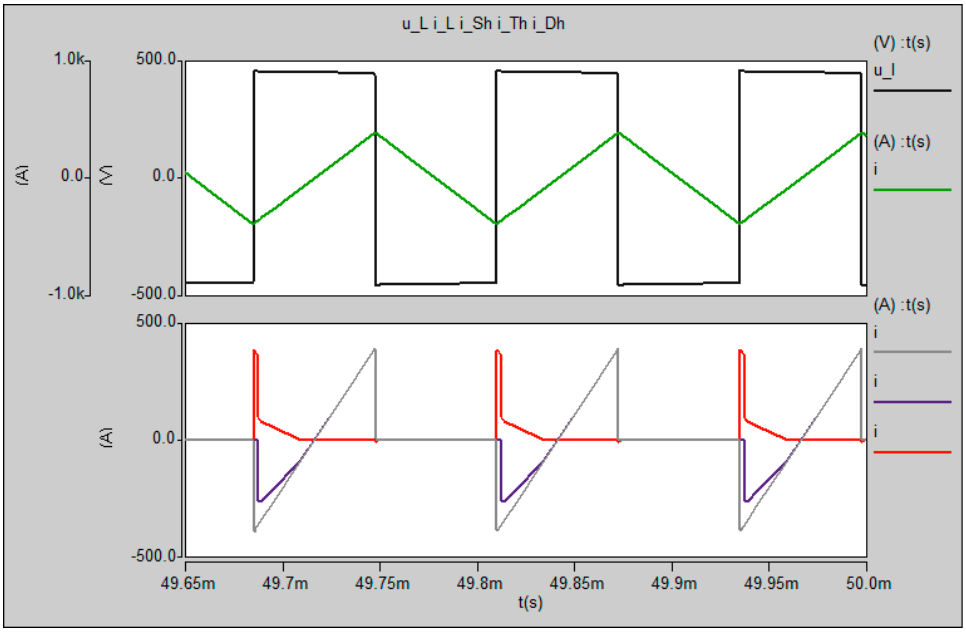
3.1. Square Wave Controlled Half-Bridge Circuit

The half-bridge circuit presented in Figure 4a may be applied to test the performance of a medium-voltage SiC power module. There is a possibility to apply an open- or closed-loop PWM control to obtain sine current in the load inductor L to acquire conditions similar to those expected in a

three-phase inverter. However, low fundamental frequency will lead to significant values of passive components. Instead, the proposed method suggests a simple square wave control at frequencies in the range of kHz to limit the necessary inductance and capacitance. At the same time, operating conditions comparable to the inverter in terms of power losses and junction temperatures can be reached. As can be seen in Figure 4b, the square wave load voltage (v_L) results in a triangle waveform of the inductor current (i_L) which is equally distributed among two switches. During the first half of the switching period, T_{SH}, the rising load current flows through the upper switch T_H/D_H, in the other half T_L/D_L are in on-state.



(**a**)



(**b**)

Figure 4. Half-bridge circuit (**a**) and basic waveforms (**b**) for square-wave operation simulated in Saber.

Behavior of the upper transistor T_H and diode D_H can be analyzed using idealized waveforms shown in Figure 5. As an initial point, the time when an opposite transistor T_L is switched off and the whole load current (amplitude I_{PK}) is commutated to the diode D_H for the dead-time period, marked as t_4, is selected. Note that the transistor and diode commutate under hard-switching conditions here. Then, starting at t_3, the transistor is switched on and conducts the reverse current together with the

diode under the assumption that the voltage drop across the on-state resistance of the transistor r_{ON} is higher than the threshold voltage of the diode V_{TO}. Over the time period t_3, the devices share current according to [10]:

$$i_T = \frac{r_D}{\Sigma r} i + \frac{V_{TO}}{\Sigma r}, \tag{9}$$

$$i_D = \frac{r_{ON}}{\Sigma r} i - \frac{V_{TO}}{\Sigma r}, \tag{10}$$

starting from I_{Ta} and I_{Da} values (see Equations (A4) and (A5) in Appendix A). This time period refers to phase II observed for a three-phase inverter in Figure 1b. Furthermore, the time of the transistor conduction, described as a duty ratio of the transistor D', may be influenced by changes of the dead-time, from $t_4 = 0$ resulting in $D' = 0.5$ until $t_4 = T_{SH}/4$ when $D' = 0.25$ and reverse conduction is disabled. Another noticeable event occurs when the load current decreases to the value:

$$I_S = \frac{V_{TO}}{r_{ON}}, \tag{11}$$

and the diode is turned-off—only the transistor is conducting reverse current (again, similarity to the area marked with the angle σ in Figure 1b can be found). Then, the load and transistor current continues to increase and finally, becomes positive after time t_2. Over last time period t_1, the transistor T_H conducts a positive load current—it ends after $T_S/4$ with a hard commutation to D_L. Then, the cycle repeats and exactly the same waveforms can be observed for the other switch during the second half of the switching period.

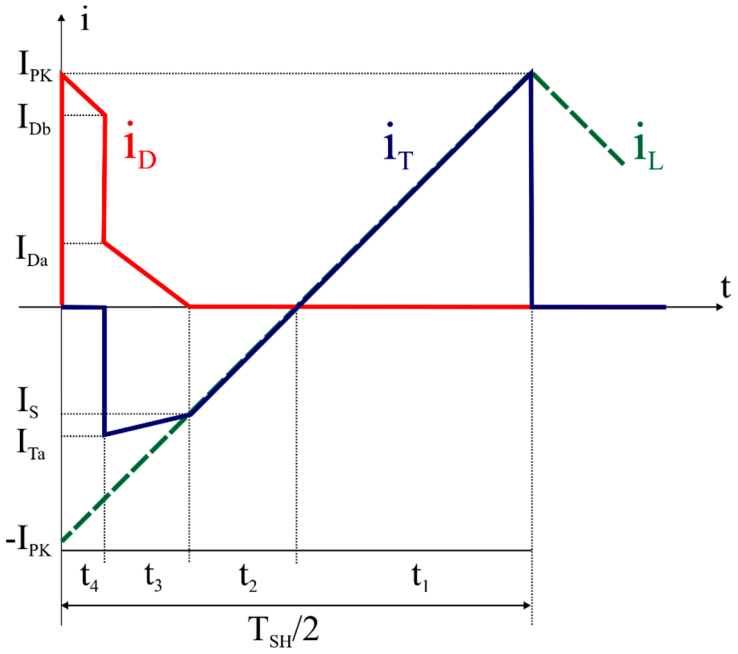


Figure 5. Square-wave-controlled half-bridge circuit: idealized waveforms of the transistor T_H (i_T) and diode D_H (i_D) current for the first half of the switching period T_{SH}.

Presented waveforms suggest that the majority of the current, and in consequence, conduction power losses, are dissipated in the transistor—similarly to a three-phase inverter. Moreover, the distribution of the losses between the two devices in the switch depends only on the amplitude of the load current I_{PK} and the parameters of the diode and transistor static characteristics (r_{ON}, V_{TO}, r_D) influenced by the temperatures. Thus, there is a chance to set a given value of the power losses in either the diode or in the transistors. Even if possible, setting the precise values in both devices requires further effort. In order to

change this distribution and push more losses from the transistor towards the diode, the simplest method is to adjust the length of the time t_4—or, in other words, the duty ratio of the transistors:

$$D' = \frac{1}{2} - \frac{t_4}{T_{SH}}, \tag{12}$$

Relations between the circuit conditions, duty ratio, static parameters of the devices and the RMS (root mean square) and average currents are collected in Appendix A, see Equations (A6)–(A15).

3.2. Method of the Inverter Power Loss Emulation

Based on the equations for the half-bridge circuit, on-state power losses in the transistor and diode may be determined (see Appendix A, Equations (A16)–(A19)). In addition, switching losses may be also easily calculated—losses occur only during the transistor turn-off process and the diode turn-on—see Figure 4. In general, the method similar to the one presented in Figure 2 may be applied here to find the power losses and junction temperatures. However, in the proposed method, the aim of such a calculation is the opposite to finding circuit conditions of the half-bridge that ensure given values of the power losses in the transistor and diode obtained from the three-phase inverter estimations. Moreover, when the cooling system is comparable to the one planned for the final inverter (3 × lower R_{THSA}), the same junction temperatures may be also obtained.

To sum up—the proposed method includes the following steps:

- Electro-thermal calculations for the selected operating point of a three-phase inverter according to the method presented in Figure 2, using Equations (1)–(8) to find power losses in transistor P_T an diode P_D.
- Calculations for the half-bridge circuit to find recommended circuit parameters of the half-bridge circuit that enables the same amount of P_T and P_D. Possibly, the same temperatures may also be planned.
- Apply the set of parameters to the test setup with the tested module and perform tests until the system reaches steady state.
- Measure power losses and (if possible) junction temperatures.
- Verify the results.

4. Experimental Verification of the Half-Bridge Circuit with 3.3 kV/450 A SiC MOSFET Modules

The analysis and simulations presented in previous section were verified by means of a series of advanced experiments including electrical and thermal measurements. The half-bridge circuit based on 3.3 kV/450 A SiC MOSFET modules from Hitachi (MSM450FS33A) equipped with self-made gate drivers with output voltage levels at +15/−9 V and supplementary protection circuits. The rest of the power circuit consists of 10 × 150 µF capacitors in the voltage divider and three reconfigurable 112 µH/500 A inductors acting as a passive load. Example of waveforms observed during an operation at 900 V and switching frequency f_{SH} = 7 kHz can be seen in Figure 6b, while specific waveforms of the transistor turn-off process are shown in Figure 6c.

One of advantages of employing the half-bridge circuit is a simple and precise measurement of the power losses at the DC input. On the other hand, the power delivered from the DC power supply is dissipated as power loss in the power modules and also load inductors. Splitting the losses between semiconductors and magnetics neither based on electrical measurements nor employing the calorimetric chamber is simple due to, among other things, wiring and isolation issues. Therefore, power losses in the SiC MOSFET modules were calculated based on measuring the temperature and flow of the coolant.

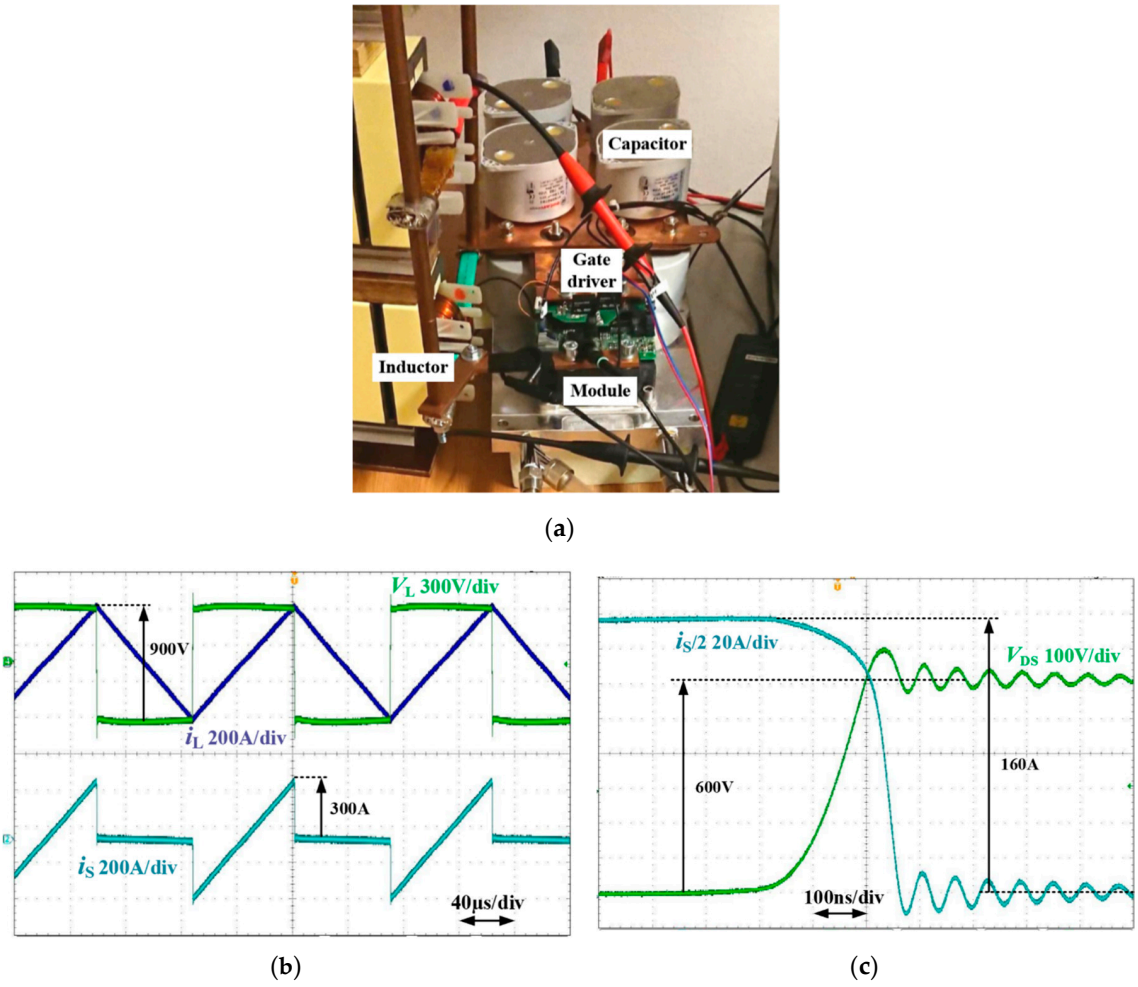
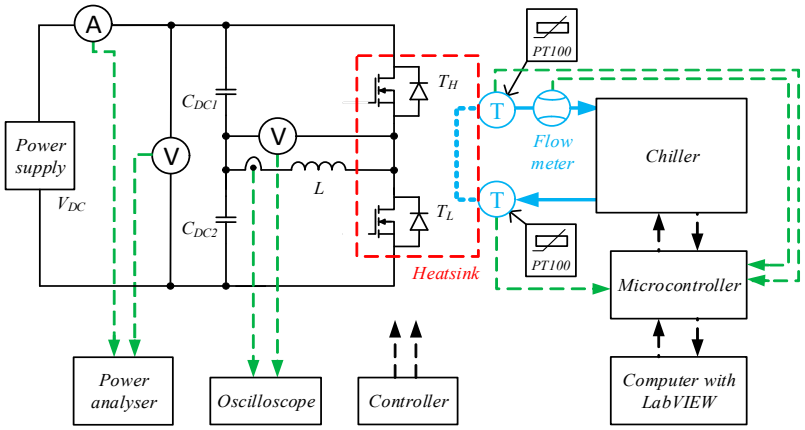


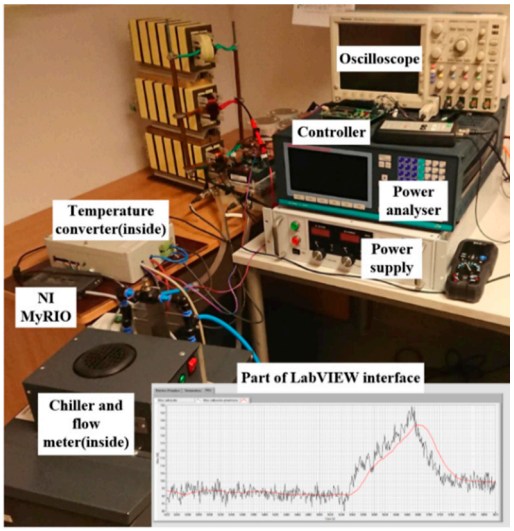
Figure 6. Photo of the half-bridge with 3.3 kV SiC MOSFET modules (**a**) and the selected waveforms recorded during the operation: inductor voltage (v_L) and current (i_L) together with the switch current (**b**) half of the upper switch (transistor) current with drain-source voltage (**c**).

The scheme and photo of the test setup is presented in Figure 7. In addition to the half-bridge circuit monitored by a high-precision power meter and digital oscilloscope, the substantial component is a setup monitoring temperature and flow of the coolant delivered to the heatsink by the chiller maintaining a constant liquid temperature in its buffer tank (+/− 0.5 °C). Power loss calculation is conducted by microcontroller NI MyRIO-1900 controlling the chiller and collecting data from the temperature converters and the flow meter. A preview of the circuit parameters along with the possibility to control the measurement process is possible via a PC with LabVIEW software (Figure 7b).

Such a setup enables testing the half-bridge circuit and measure the power losses in the SiC MOSFET modules and can be applied to validate equations from Section 3 at various operating points. In order to avoid damaging the modules and obtain precise results, a special procedure was used for each operating point defined by means of input voltage V_{DC}, inductance L, switching frequency f_{SH} and duty ratio D. At first, the calculation is performed using MATLAB to check if the module is in safe operation area by means of current, voltages, power loss and junction temperatures. Then, the half-bridge is powered and operates at selected conditions just to perform the switching energy measurements (E_{offT} and E_{onD}), which are applied to repeat MATLAB calculations with experimental results. In the next step, the half-bridge circuit is pushed into continuous operation for at least 30 min to reach the thermal steady state and conduct the complete cycle of the thermal measurements. Finally, the results from the calculations can be compared with the obtained power loss value.



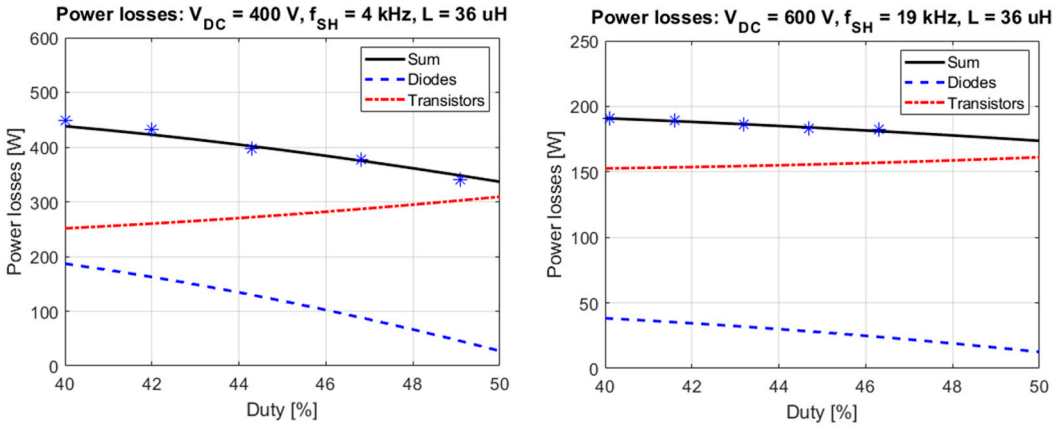
(**a**)



(**b**)

Figure 7. Scheme (**a**) and photo (**b**) of the half-bridge measurement setup.

After checking different operating points, the procedure described above was used to verify the characteristics of the power losses versus duty ratio D'. Other parameters (V_{DC}, L and f_{SH}) were set as constant. It is noteworthy that this parameter shows slight influence on the total amount of power losses. Nevertheless, it will also decide about the split between diode and transistor. To illustrate this issue, a series of calculations using the procedure presented in Figure 2 was conducted in MATLAB for an exemplary case (V_{DC} = 400 and 600 V, L = 36 µH, and f_{SH} = 4 and 19 kHz)—see Figure 8. As expected, the decrease in the duty ratio D' leads to an increased current in the diode and elevated losses, and at the same time losses in MOSFETs slightly drop. The results of experiments presented in Figure 8 and in Table 1 are consistent with advanced electro-thermal calculations. Operating points were chosen to test the different values of voltage, inductance and switching frequency, as well as different power levels. For all cases, the total measured losses change with the duty ratio and the maximum relative error ($\max\delta_P$) was found to be below 4%. This means that the proposed method shows very good precision and can be implemented in validation of the power modules at requested power levels including an accurate split of power losses between the transistors and diodes.



(**a**) (**b**)

Figure 8. Power losses in the half-bridge: transistors (red), diodes (blue) and sum of power losses in the module (black) obtained from calculations in MATLAB and experiments (stars) shown for two cases: V_{DC} = 400 V, f_{SH} = 4 kHz (a) and V_{DC} = 600 V, f_{SH} = 19 kHz (b).

Table 1. Results for all measurement series carried out for different operating points.

Operating Point					Power Comparison		
V_{DC} (V)	L (µH)	f_{SH} (kHz)	I_{PK} (A)	ΔD (%)	ΔP_{calc} (W)	ΔP_{meas} (W)	max|δ_P| (%)
400	36	4	348	49.1–40	348–438	340–448	2.3
400	36	7	192	48.9–40.5	154–181	154–187	3.3
500	36	10	171	48–41.6	184–202	186–210	4
500	56	10	114	48–41.6	106–117	102–117	3.8
600	36	7	296	48.9–40.5	390–449	391–454	2.7
600	36	13	159	48–41.7	227–243	222–245	2.2
600	36	19	104	46.3–40.1	181–191	182–191	0.6

5. Experimental Validation of Power Loss in Three-Phase Inverter Using the Half-Bridge Circuit

In the final section, an example of power loss validation is presented by means of experiments in the half bridge circuit. In reference to the datasheet parameters of the available power modules (MSM450FS33A), a case of the three-phase inverter rated at 220 kVA was investigated for input voltage V_{DC} = 1500 V, switching frequency f_S = 2.5 kHz, dead-time period T_{DT} = 4 µs and unity power factor. According to the procedure described in Section 3.2, the first step is to calculate the power losses in transistors and diodes—here the characteristics presented in Figure 3b were used to find that P_T = 170 W and P_D = 25 W. It is noteworthy that the accuracy of calculations has been improved as a result of applying double pulse measurements in MATLAB [37] instead of datasheet values.

The next step was to find a set of half-bridge circuit parameters (input voltage V_{DC}, load inductance L, switching frequency f_S and duty ratio D) enabling the same values of losses in transistors and diodes. Theoretically, the equations presented in Section 3 and Appendix A offer a wide range of possibilities in terms of electrical parameters as the required P_T and P_D can be obtained in an infinite number of settings. However, the limitation is a maximum DC voltage (<1800 V for tested modules) and the switching frequency, which is restricted bythe delays in the gate driver circuit. Nonetheless, the main issue comes in a form of load inductors accessibility—here three inductors were available. Another observation is that the total losses are influenced by voltage, inductance and switching frequency while duty ratio decides about the split between the diode and the transistor. Taking the above into account, the following parameters were proposed to test the single phase leg in the half-bridge circuit with inductive load: V_{DC} = 600 V, L = 36 µH, f_S = 7 kHz and D = 48.9%. Calculations in MATLAB confirmed that for assumed heatsink parameters (R_{THSA} = 35 K/kW), expected levels of P_T and P_D will be dissipated in the SiC MOSFETs and Schottky diodes of the power module.

Then, a series of laboratory measurements were performed using the setup described in Section 4, for the assumed parameters the RMS current in the load inductors was measured to be 172 A RMS (298 A peak). It corresponds to 1032 W observed at the input by a precise power meter. This value is rather useful for overall system monitoring due to unknown loss in the inductors. The electro-thermal measurements confirmed that the power losses in the whole power module (two transistors and two diodes), further dissipated in the liquid-cooled heatsink, were at the level of 391 W (Figure 9). During such a test, it is not possible to find the split of the power losses between the diode and the MOSFET, however, further measurements of total losses for decreased duty ratio (Figure 9) were in very good agreement with the calculations. Thus, it is very likely that not only the assumed amount of losses was applied to the whole power module but also specifically to the following transistors and diodes to obtain the same electrical and thermal conditions as in a three-phase inverter.

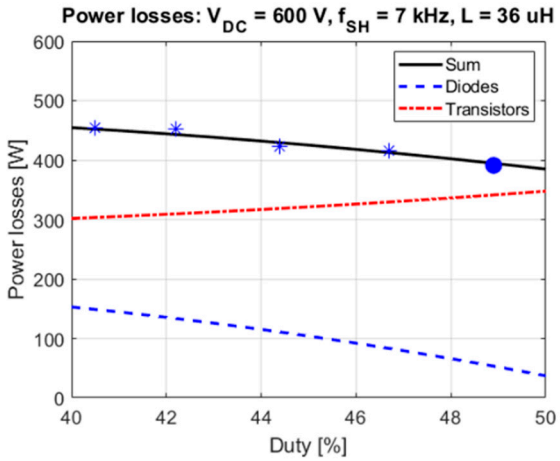


Figure 9. Power losses in the half-bridge: transistors (red), diodes (blue) and the sum of power losses in the module (black) obtained from calculations in MATLAB and experiments (blue dot and stars).

6. Conclusions

In response to a series of problems in proper design of three-phase inverters with medium-voltage SiC MOSFET modules, a new method of power losses validation was presented in this paper. The method is based on accurate equations describing on-state losses in a three-phase inverter, and also, a half-bridge circuit loaded with an inductor. Combined electro-thermal calculations are applied to estimate power losses in the transistors and diodes of the inverter and then, to find suitable circuit parameters of the half-bridge circuit appropriate to emulate these conditions. The experimental part of the method is reduced only to tests of such a circuit with simple square-wave control. Huge amounts of reactive power circulate between DC-link capacitors and inductors to apply the assumed amount of power losses. It is important that the provided equations enable the precise emulation of power losses in the module and also in specific devices—this feature has been confirmed via a series of measurements using 3.3 kV/450 A SiC MOSFET. The same module was applied, in addition to an inductive load and two sets of DC-link capacitors, to validate the case of a 220 kVA inverter. What is especially valuable, is that the necessary power supply is limited. Slightly above 1 kW is sufficient to test a single power module operating under conditions comparable to a full scale inverter. In addition to the simple setup reducing the cost, this may be counted as a major advantage of the proposed method.

Author Contributions: J.R. proposed the main concept and the methodology. H.S. was the main contributor with regard to the theoretical analysis and the experimental setup. R.K., P.T. and G.W. contributed to the experimental study and further data analysis. Supervision, project administration, funding acquisition—J.R. All authors have contributed to the writing of the paper. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Assuming the linear rise of the load current:

$$t_2 = \frac{V_{\mathrm{TO}} T_{\mathrm{SH}}}{4 I_{\mathrm{PK}} r_{\mathrm{ON}}}, \tag{A1}$$

$$t_3' = \frac{T_{\mathrm{SH}}}{4}\left(4D' - 1 - \frac{V_{\mathrm{TO}}}{I_{\mathrm{PK}} r_{\mathrm{ON}}}\right), \tag{A2}$$

Transistor and diode current can be expressed as

$$I_{\mathrm{Db}} = I_{\mathrm{PK}}(4D' - 1), \tag{A3}$$

$$I_{\mathrm{Da}} = \frac{r_{\mathrm{ON}} I_{\mathrm{PK}}(4D' - 1) - V_{\mathrm{TO}}}{\sum r}, \tag{A4}$$

$$I_{\mathrm{Ta}} = \frac{r_{\mathrm{ON}} I_{\mathrm{PK}}(4D' - 1) + V_{\mathrm{TO}}}{\sum r}, \tag{A5}$$

This leads to equations describing RMS currents of the transistor:

$$I_{\mathrm{T1rms}} = \frac{I_{\mathrm{PK}}}{\sqrt{12}}, \tag{A6}$$

$$I_{\mathrm{T2rms}} = \sqrt{\frac{t_2}{3T_{\mathrm{SH}}}} I_{\mathrm{S}} = \frac{1}{2}\sqrt{\frac{V_{\mathrm{TO}}^{\,3}}{3 I_{\mathrm{PK}}\, r_{\mathrm{ON}}^{\,3}}}, \tag{A7}$$

$$I_{\mathrm{T3rms}} = \sqrt{\frac{t_3}{3T_{\mathrm{SH}}}\left(I_{\mathrm{Ta}}^{\,2} + I_{\mathrm{Ta}} I_{\mathrm{S}} + I_{\mathrm{S}}^{\,2}\right)}, \tag{A8}$$

And the diode:

$$I_{\mathrm{D3rms}} = \sqrt{\frac{t_3}{3T_{\mathrm{SH}}}} I_{\mathrm{Da}}, \tag{A9}$$

$$I_{\mathrm{D3AVG}} = \frac{t_3}{2T_{\mathrm{SH}}} I_{\mathrm{Da}}, \tag{A10}$$

$$I_{\mathrm{D4rms}} = \sqrt{\frac{t_4}{3T_{\mathrm{SH}}}\left(I_{\mathrm{PK}}^{\,2} + I_{\mathrm{PK}} I_{\mathrm{Db}} + I_{\mathrm{Db}}^{\,2}\right)}, \tag{A11}$$

$$I_{\mathrm{D4AVG}} = \frac{t_4}{2T_{\mathrm{SH}}}(I_{\mathrm{Db}} + I_{\mathrm{PK}}), \tag{A12}$$

$$I_{\mathrm{Trms}} = \sqrt{(I_{\mathrm{T1rms}})^2 + (I_{\mathrm{T2rms}})^2 + (I_{\mathrm{T3rms}})^2}, \tag{A13}$$

$$I_{\mathrm{DAVG}} = I_{\mathrm{D3AVG}} + I_{\mathrm{D4AVG}}, \tag{A14}$$

$$I_{\mathrm{Drms}} = \sqrt{(I_{\mathrm{D3rms}})^2 + (I_{\mathrm{D4rms}})^2}, \tag{A15}$$

$$P_{\mathrm{CT}} = I_{\mathrm{Trms}}{}^2 r_{\mathrm{ON}}, \tag{A16}$$

$$P_{\mathrm{CD}} = V_{\mathrm{TO}} I_{\mathrm{DAVG}} + I_{\mathrm{Drms}}{}^2 r_{\mathrm{D}}, \tag{A17}$$

$$P_{\mathrm{SWT}} = \frac{E_{\mathrm{offT}}}{\mathrm{T_{SH}}}, \tag{A18}$$

$$P_{\mathrm{SWD}} = \frac{E_{\mathrm{onD}}}{\mathrm{T_{SH}}}, \tag{A19}$$

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3.3 Medium Voltage Power Switch in Silicon Carbide—A Comparative Study [P3]

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Medium Voltage Power Switch in Silicon Carbide–A Comparative Study

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ABSTRACT This paper discusses various solutions of energy conversion in medium voltage using power switches in Silicon Carbide (SiC) technology. In particular, a comparative study is focused on four different variants of an inverter phase leg operating at 1.5 kV DC, which has not been presented in the literature yet. The first one is based on a standard two-level half-bridge built from a 3.3 kV SiC MOSFET power module rated at 450 A. Then, the two-level solution with series-connected devices inside 1.2 kV/450 A power modules is taken into account. Finally, a flying-capacitor phase leg also based on the same 1.2 kV devices is investigated in two different modes: a standard three-level operation and quasi-two-level mode with a significantly reduced capacitor. The presented study is founded on in-depth experiments: all four phase legs were designed, built, and tested in the laboratory. All versions were connected in a half-bridge configuration with an inductive load. Tests were conducted under identical conditions to test the overall performance and switching behavior for various gate resistances. In addition, different aspects are analyzed and compared in this paper, including parasitics, cooling performance, gate drivers and layout considerations, providing selection guidelines for power switches with SiC power devices in medium voltage power electronics applications.

INDEX TERMS Medium voltage, power converters, power electronics, power MOSFETs, silicon carbide.

I. INTRODUCTION

Silicon Carbide power devices have a substantial impact on power electronics [1]–[3] employed in energy conversion and management systems, as they offer lower on-state resistances and higher switching speeds in comparison to Silicon (Si) counterparts, and more efficient or/and more compact power converters can be designed [4]. This conclusion may be drawn from a number of research works and industrial applications in various fields where mostly low voltage (650 V to 1200 V) SiC diodes and transistors can be found. In the case of devices developed to operate at medium voltages, an influence of the new technology may be even more significant as SiC MOSFETs reach blocking voltages not available for Si technology [5], [6] and can replace Si IGBTs. Thus, in many applications, SiC transistors enable operation at higher DC voltages [7], [8], and complex multilevel converters structures required for Si devices can be replaced by two-level ones. At the same time, SiC power devices can compete against Si IGBTs rated at 1700, 3300, and 6500 V in applications where the switching frequency is an essential factor. As the switching energies of SiC MOSFETs with a comparable current rating are usually a few times lower, the outcome of this competition is not hard to be predicted. On the other hand, the cost of SiC power devices, especially those rated at medium voltage, is much higher than Si counterparts. All in all, SiC technology offers new possibilities, but it is not necessarily advantageous in all applications [9]. Another issue is that SiC power devices are still a new technology at medium voltage and, in the authors opinion, a discussion on the most beneficial way to use them is still not over. At the moment at least four approaches can be taken into account.

As mentioned above, using medium voltage (MV) rated SiC devices in simple two-level topologies [1], [10], [11] is the most obvious as such devices are available. Unfortunately, the cost is a limiting factor, and in this basic case, it has

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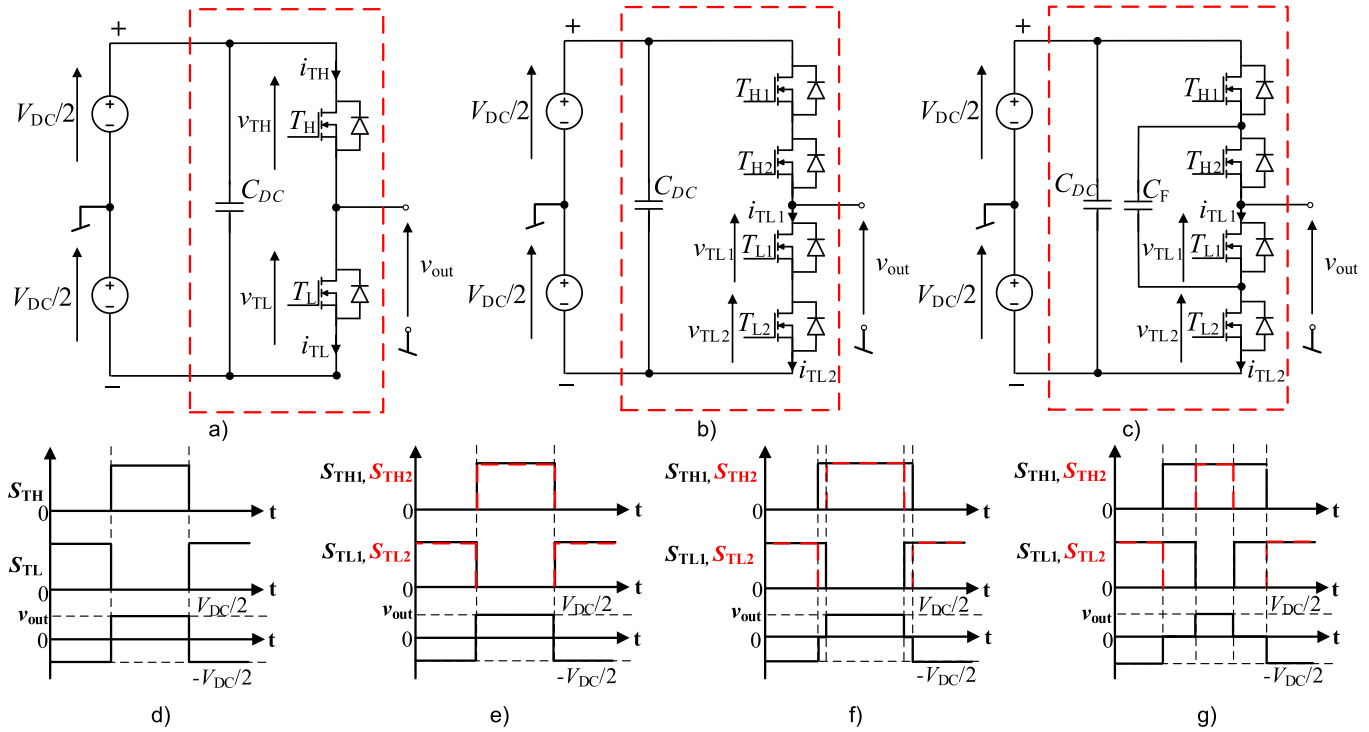

FIGURE 1. Circuit schemes for the four different variants of medium-voltage phase-leg based on SiC power devices: two-level with medium voltage devices (2LMV) scheme (a), idealized waveforms (d); two-level series-connected with low voltage devices (2LSC) scheme (b), idealized waveforms (e); quasi-two-level flying capacitor with low voltage devices (2LFC) scheme (c), idealized waveforms (f); three-level flying capacitor with low voltage devices (3LFC) scheme (c), idealized waveforms (g).

to be balanced with the system's simplicity. On the other hand, many works have been done on series-connection of SiC MOSFETs [12]–[18], and a power switch based on less expensive low voltage devices is also an attractive solution. However, the drawback of this approach is higher complexity. Moreover, there are no power modules with series-connected devices, therefore, the layout is more challenging. Finally, additional effort is also required in terms of the control system. Thus, an interesting alternative to series-connection of SiC MOSFETs is a multilevel flying capacitor (FC) inverter operating in quasi-two-level (Q2L) mode where middle states are used only for a very short time, and thus the flying capacitor is very small [19]–[23]. Finally, it is also possible to take a well-known path and employ any multilevel topologies using low-voltage SiC power devices [4], [24]–[26]. All these approaches were thoroughly discussed in the literature separately, but a suitable multicriterial comparison, based on experimental models and test, for MV converters employing SiC power devices was missing.

That is why this paper contains a comparative study of four options mentioned above, with circuit schemes and idealized operating waveforms shown in Fig. 1, starting from a two-level with medium voltage devices (2LMV, Fig. 1a), through a two-level with series-connected transistors (2LSC, Fig. 1b), a three-level flying-capacitor in quasi-two level mode (2LFC – Fig. 1c) to a standard three-level flying-capacitor (3LFC– Fig. 1c as well). All four cases are explained briefly in section II, but here, only general description of the specific approaches, required to understand the basic operation principles, is presented. The idea of this paper is to provide a general comparison useful for designers and researchers for initial choice of an appropriate method to create SiC power switches in medium voltages for a specific application. For more thorough analysis with detailed theoretical description, after the initial choice, the authors recommend to get acquainted with the referenced literature. This work's essence are physical models (section III) and experiments on phase-legs based on 450 A-rated SiC MOSFETs operating at 1.5 kV DC (section IV) along with a thorough discussion and the comparison of the presented approaches shown in section V, while the paper is concluded in section VI.

II. FOUR APPROACHES TO MEDIUM VOLTAGE ENERGY CONVERSION WITH SIC POWER DEVICES

A. TWO-LEVEL WITH MEDIUM VOLTAGE DEVICES (2LMV)

The basic approach to employ SiC power devices in the medium voltage range is to directly apply single MV transistors as the power switches, as shown in Fig. 1a. The most considerable merit of such a method is the simple structure – a single power module per converter leg is used. Therefore a simple control can be applied (Fig. 1d). The whole leg is compacted within a single power module, thus leading to a more straightforward layout of the power circuit and high cooling capabilities. However, as high *dv/dt* ratios characterize such

power devices, driver design is not trivial [14], [27]–[29]. Finally, even though SiC power devices reaching as high as 15 kV have been shown in the literature [30], commercially available transistors with reasonable current ratings are still limited to 3.3 kV, and thus such a simple approach is not applicable for higher voltage ratings and more sophisticated options have to be considered. Last but not least, the cost of such devices is still high.

B. TWO-LEVEL WITH SERIES-CONNECTED LOW VOLTAGE DEVICES (2LSC)

Series connection of low-voltage transistors is a well-known method to construct switches capable of blocking higher voltages [31]. In general, this approach is also based on a simple structure. A number of series-connected SiC MOSFETs are used instead of a single transistor, as shown in Fig. 1b. In the discussed case, two transistors per switch are considered, as this provides the possibility to have a transistor pair within a half-bridge power module. Thus the whole leg consists of two such half-bridge modules, however, the best option would be a power module with series connected chips. In an idealized case, each series-connected device should receive the same control signal as shown in Fig. 1e, and the leg output voltage v_{out} is identical to the 2LMV case. However, unbalanced voltage distribution among the power devices in the stack leads to a more complex structure of the series-connected system, either through adding supplementary circuits or altering the control scheme, depending on the voltage balancing method used. This is especially prominent for SiC transistors, where the switching speed is very high, and the impact of parasitic parameters and mismatches, leading to voltage imbalances, is higher than in conventional Si power devices [12]. In order to attain safe operating conditions for the series-connected power devices auxiliary structures in the form of simple passive systems (e.g., snubbers or clamping circuits) [31] or more sophisticated active systems, often including additional measurement systems, for example, based on active gate driving or active gate delay methods [13]–[15] have to be employed.

C. QUASI-TWO-LEVEL WITH LOW VOLTAGE DEVICES (2LFC)

Another approach to employ low-voltage SiC MOSFETs in the MV range is to use the well-known multilevel flying capacitor converter (FCC) structure, showcased in Fig. 1c, in a quasi-two-level control mode [19] – see Fig. 1f – which results in an output voltage shape nearly identical to the conventional two-level approaches. Such a method can, in fact, be recognized as an alternative approach to series-connection of transistors, in which a small flying capacitor is an additional component that assures proper voltage distribution among the power devices. While the general operating sequences are akin to a conventional multilevel FCC, the difference is visible in the length of the three-level states – in the Q2L mode, these are employed for very brief moments, usually less than 1% of the switching period, just to balance the voltage among the transistors. Thus, the flying capacitor is very small. However, to sustain proper voltage distribution among the transistors, balanced flying capacitor voltage is also required, which necessitates alterations in the switching pattern and usually requires additional measurement circuits.

D. THREE-LEVEL WITH LOW VOLTAGE DEVICES (3LFC)

Finally, employing multilevel converters is also a viable and well-researched approach. A large variety of different topologies may be named, each with its advantages and disadvantages, most notably, neutral-point-clamped, active neutral-point-clamped, T-type, flying capacitor, as well as cascaded and modular structures [32]. Here, the flying capacitor-based system (Fig. 1c) was chosen because of the similarities to the 2LFC circuit. In the conventional, multilevel-operated FCC, the three-level states are employed

TABLE 1. Parameters of the experimental models for each of the approaches.

Parameter	2LMV	2LSC	2LFC	3LFC
Power module	MSM450FS33A	CAB450M12XM3	CAB450M12XM3	CAB450M12XM3
Rated Drain-Source Voltage [V]	3300	2400 (1200)	2400 (1200)	2400 (1200)
Drain Current [A]	450	450	450	450
On-state resistance @ 25°C [mΩ]	5.3	5.2 (2.6)	5.2 (2.6)	5.2 (2.6)
Cooling plate area [cm^2]	140	84.8 (42.4)	84.8 (42.4)	84.8 (42.4)
Internal inductance [nH]	10	13.4 (6.7)	13.4 (6.7)	13.4 (6.7)
Switching energy per pulse rated to switched power [mJ/kW]	802	156 (78)	156 (78)	156 (78)
Internal gate resistance [Ω]	2.6	2.5	2.5	2.5
Cost, price [$]	6000	1700 (850)	1700 (850)	1700 (850)
Gate driver	Self-made	Self-made	MS2K8W9A-17	MS2K8W9A-17
Additional components	none	Active voltage balancing circuitry, including 3 voltage measurements	820 nF flying capacitance, built on 2212 C0G SMD, 2 volt. measurements	300 µF flying capacitance, 2 x DUCATI 416890752, 2 volt. measurements

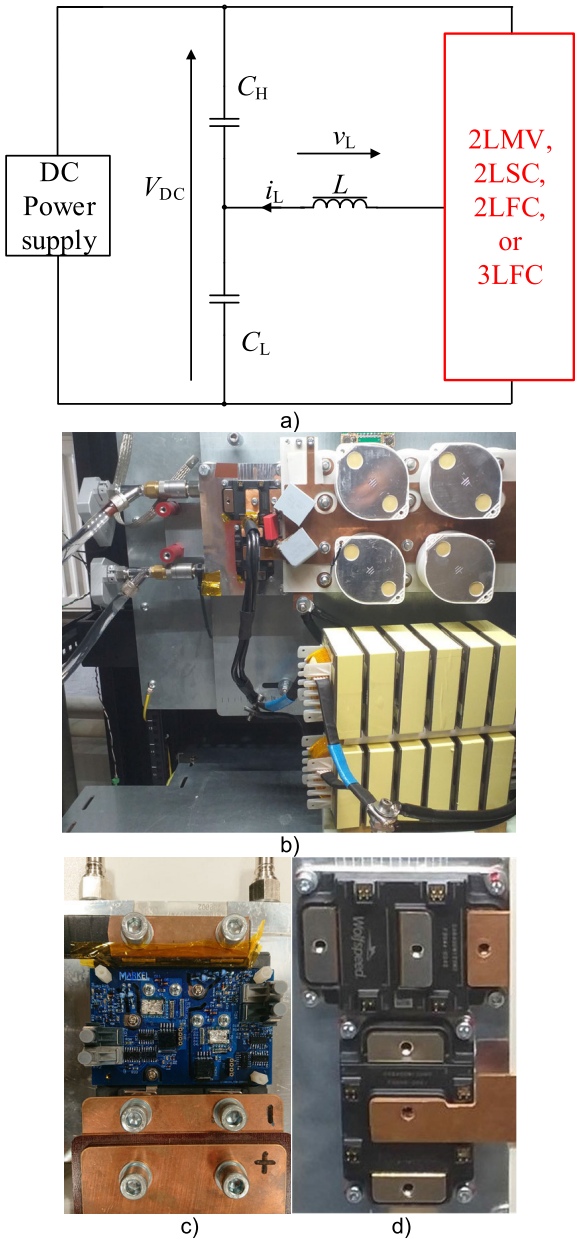

FIGURE 2. Scheme of the half-bridge with inductive load test-setup (a), general photo of the half-bridge circuit (b), 2LMV variant (c), setup for 2LSC, 2LFC, 3LFC (d).

for a substantial amount of time, as depicted in Fig. 1g. Therefore, the flying capacitor is quite bulky, as it has to sustain high values of the current. On the other hand, three-level output leg voltage v_{out} provides a lower harmonic component, and smaller filtering inductance may be applied compared to the discussed two-level options.

III. EXPERIMENTAL SETUP

As a basis of the comparisons, four experimental models rated at 1.5 kV DC were designed, constructed, and tested – see the parameters in Tab. 1, where the values in the brackets indicate the parameters for one device. The test setup was in half-bridge topology with an inductive load (roughly 55 μH/400 A choke), so only power losses of the system had to be supplied from the DC source, as presented in the circuit scheme in Fig. 2a, where the red box corresponds to the specific approach showcased in the scheme in Fig. 1a to 1c. DC-link capacitor bank was built from 5 $\times$ 150 μF capacitors connected in parallel per half of the DC-link (see Fig. 2b – photo of the test circuit) and used for each approach, so that identical electrical conditions from DC-side could have been obtained. For the 2LMV approach, the 3.3 kV, 450 A SiC MOSFET module (MSM450FS33A [33] – Fig. 2c) was selected, the other three options used 1.2 kV modules with the same current rating (CAB450M12XM3 [34] visible in Fig. 2d), as unfortunately, the commercially available 1.7 kV SiC power modules are not as highly-performant, mostly due to enlarged parasitic inductances and high power loss. Moreover, the heatsink and the liquid cooling system was identical for all the setups. Therefore, the thermal conditions and temperatures for different approaches were strictly based on the individual performance of each system.

The design for 2LMV is the most compact as there is no additional circuitry in this approach. Moreover, the parasitic inductance of the switching loop is minimal due to low internal inductance and a simple layout. On the contrary, the power circuits for the other three approaches with two modules are more complex and contain higher parasitic inductance. The majority of the layout is the same, however, extra components, for instance, flying capacitors, differ for 2LFC and 3LFC. In particular, two 150 μF capacitors connected in parallel were applied for 3LFC to obtain the same voltage ripples as in 2LFC (820 nF, built from 2212 C0G SMD capacitors). These capacitors contribute to an increased inductance of the switching loop. In all three cases, the performance could be improved if a specific, dedicated power circuit for each option existed, including DC-link capacitor selection. Additional control circuitry was also different among the approaches as presented in Tab. 1. The 2LSC was based on active gate delay voltage balancing, executed within the gate driver. The operation principle is as follows: the master control sends switching signals as to a conventional single-module half-bridge. Then, each gate driver for the power module, based on DC and one transistor from switch voltage measurement, employing a closed-loop control algorithm implemented into the TMS320F28069 microcontroller included in the gate driver, adds very short delays, in the span of single nanoseconds with a resolution of 150 ps, to the appropriate gate signals to balance the voltage among the transistors in the stack [15]. In the 2LFC approach, the proper voltage distribution among the transistors is ensured with a closed-loop control based on DC and flying capacitor voltage measurement [23], and a hysteretic regulator is also employed. Finally, a standard, less challenging method was applied to the 3LFC.

IV. EXPERIMENTS

The main goal of the performed experiments was to test, validate and compare all developed models and methods under the same conditions close to the real operation of

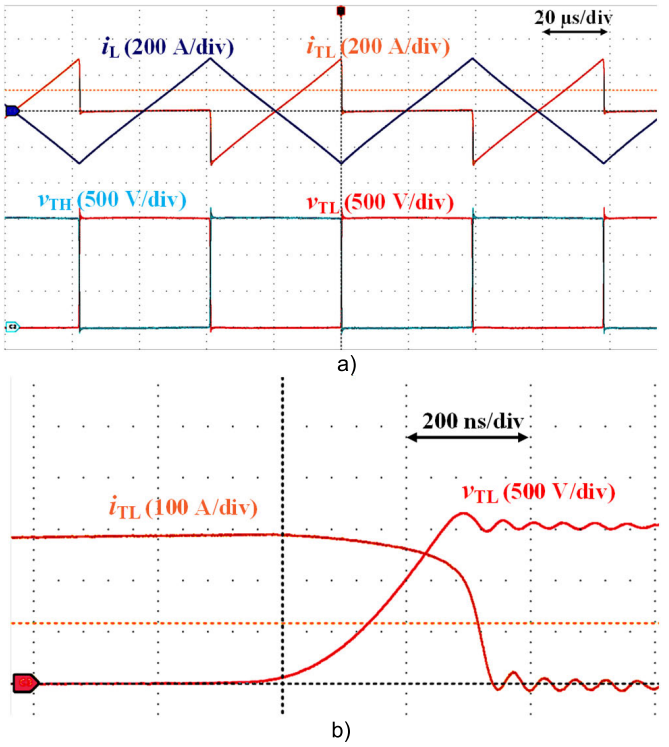

FIGURE 3. Exemplary results for the 2LMV approach performed at 1500 V, 1.6 Ω gate resistance, and roughly 295 A switched current: a) general view, b) turn-off process.

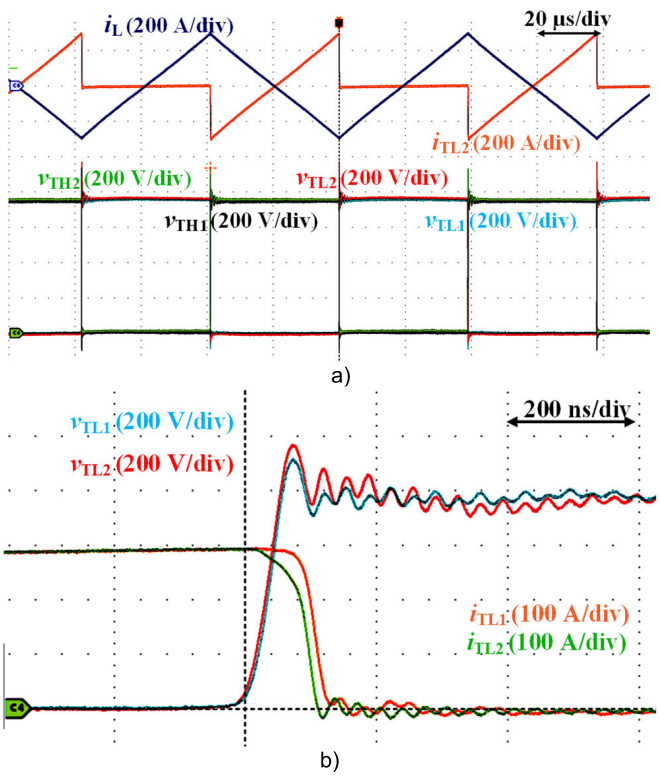

FIGURE 4. Exemplary results for the 2LSC approach performed at 1500 V, 1.6 Ω gate resistance, and roughly 295 A switched current: a) general view, b) turn-off process.

the medium voltage converters, including the assessment of the semiconductor power losses, further used for comparison. Thus, all variants acting as 1.5 kV-rated half-bridges were loaded with identical inductors (Fig. 2b), and a simple square wave control with adjustable frequency was applied. This method enables operation at high voltages and currents (1.5 kV/300 A) with limited power from the DC supply as energy is circulating between load inductor and DC-link capacitors. All in all, current and voltage waveforms presented in Fig. 3a to Fig. 6a for all four approaches are comparable while switching processes illustrated in Figs. 3b to 6b show differences.

At first, Fig. 3 showcases the exemplary results for the 2LMV approach using a single 3.3 kV power module at 12.8 kHz switching frequency. Specific waveforms shown in Fig. 3a confirm the correct operation of the circuit with square wave control – triangle shape of the load current i_L and its part contributing to the current of the upper transistor i_{TL}. Only the turn-off process occurs in such an operation, as shown in Fig. 3b, taking over 300 ns ($R_G = 1.6\ \Omega$). The advantage of the reduced parasitic inductance is the low overshoot of the drain-source voltage, which reaches a maximum of 1656 V (approx. 10% over DC-link voltage). The turn-off energy calculated from this waveform equals to 61.4 mJ – see Tab. 2.

Next, Fig. 4 presents the waveforms recorded at the same conditions but for the 2LSC approach with active voltage balancing. Since this is still a two-level topology as well, the inductor current behaves identically as in 2LMV (Fig. 4a). As shown in Fig. 4a and in the zoomed view in Fig. 4b, the balancing loop works properly, and the voltage is evenly distributed across two transistors, leading to safe operating conditions. For the 1.2 kV transistors, the switching speed is much higher, and the parasitic inductance effect is more severe, leading to an overshoot of 22% and maximum drain-source voltage of 915 V at T_{L2} accompanied by

TABLE 2. Results from the experiments performed at 1500 V DC voltage and minimal gate resistance.

Approach	f_{SW} [kHz]	$I_{L(RMS)}$ [A]	$I_{T(switched)}$ [A]	E_{OFF} [mJ]	P_{OFF} [W]	P_C [W]	T_J [°C]
2LMV, $R_G = 1.6\ \Omega$	12.8	164	291	61.4	786	75	60
2LSC, $R_G = 1.6\ \Omega$	12.8	166	294	32.3	414	74	41
2LFC, $R_G = 1.6\ \Omega$	12.8	166	297	33.6	430	74	42
3LFC, $R_G = 3.3\ \Omega$	6.8(12.8)	231	292	45.2	308(578)	134	38(55)

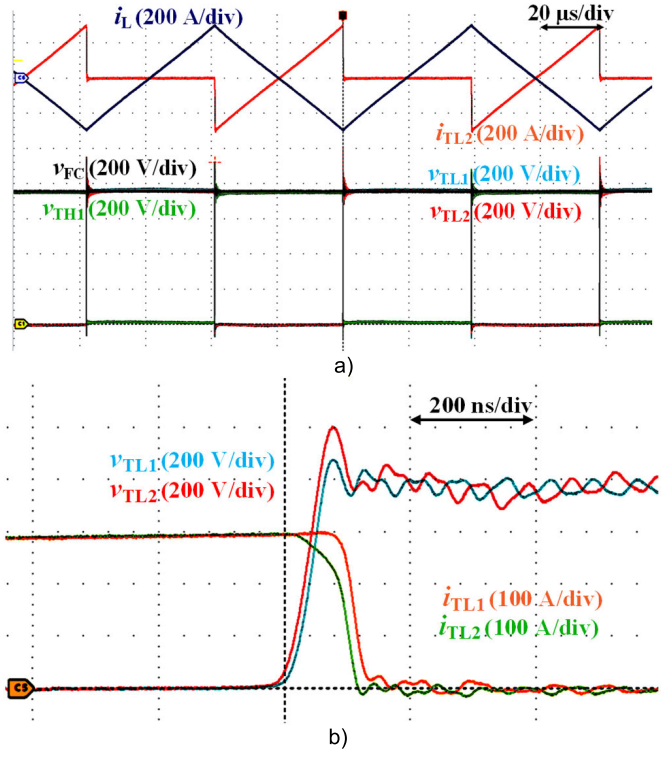

FIGURE 5. Exemplary results for the 2LFC approach performed at 1500 V, 1.6 Ω gate resistance, and roughly 295 A switched current: a) general view, b) turn-off process.

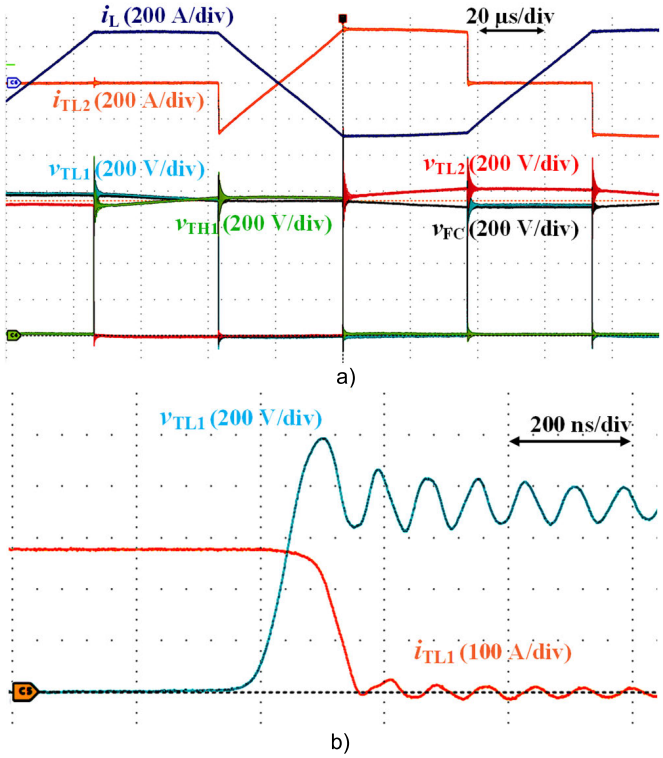

FIGURE 6. Exemplary results for the 3LFC approach performed at 1500 V, 3.3 Ω gate resistance, and roughly 295 A switched current: a) general view, b) turn-off process.

high-frequency oscillations. However, the total energy in the two transistors is equal to 32.2 mJ (@$R_G = 1.6\ \Omega$) – roughly half of the value measured for the 3.3 kV counterpart (Tab. 2).

The results for the 2LFC approach are shown in Fig. 5. Since the Q2L method can be recognized as just another method to connect transistors in series, the general waveforms are similar to 2LSC. However, the current path length is slightly enlarged due to an additional component in the power circuit, namely, the small flying capacitor, and the voltage overshoot was higher as well, reaching approximately 34% with a maximum voltage of 1007 V. Slight increase in the measured turn-off energy is also observed in Tab. 2.

Finally, Fig. 6 showcases the results for the 3LFC method. Since the operation is different from the previous approaches, the inductor and transistor current shapes resemble a trapezoidal form due to extended three-level states (Fig. 6a). This also resulted in different RMS current values as well as the operating frequency. In order to compare this method with other approaches, it was decided to set the operating point so that the switched transistor current was identical as for the different techniques. Due to the additional inductance introduced by the large flying capacitor, the system with 1.6 Ω gate resistance was unstable. Thus, the observed waveforms are shown in Fig. 6b for higher $R_G = 3.3\ \Omega$, the drain-source voltage reached a maximum value of 1148 V, resulting in an overshoot at 53%. In addition to severe oscillations, a rise of the switching energy to 45.2 mJ is observed (Tab. 2). However, this is also impacted by enlarged gate resistance

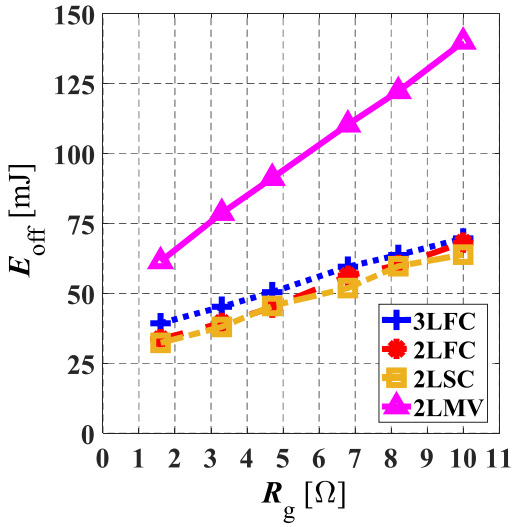

FIGURE 7. Comparison of turn-off switching energies per switch for various approaches in function of gate resistance. Results based on experimental tests performed at 1500 V and roughly 295 A switched transistor current.

compared to other cases. Based on the measured waveforms, estimations of power losses and junction temperatures were also conducted and are presented in the same Table. They confirm the best performance of the 2LSC approach, highly comparable to the 2LFC variant. The 3LFC method cannot be directly compared at the same switching frequency, as for the same inductance, the power level shifts. Therefore, values in the brackets refer to a possible 12.8 kHz case, mimicking

TABLE 3. Comparison of various parameters for all four approaches to medium voltage power switch realization.

Parameter	2LMV	2LSC	2LFC	3LFC
Waveforms quality	medium	medium	medium	high
Parasitic inductances	very low	medium	medium to high	high
Power losses	high	low	low	low to medium
Cooling performance	high	medium	medium	medium
Gate drivers	complex	standard	standard	standard
Auxiliary units	none	complex	required	required
Reliability	high	low	low to medium	medium
Cost	very high	low	low	low
Start-up	none	required	required	required

the frequency for two-level approaches used for comparison, where the switching energy loss was scaled using larger frequency. All in all, it seems that this approach is less favorable in terms of power loss, but the worst case is 2LMV.

In the further measurements, the same tests were performed but for higher values of the gate resistors – see results in Fig. 7. Moreover, it is worth noting that the internal gate resistances for both modules were highly comparable (2.5 Ω vs 2.6 Ω) and thus omitted in the comparison. With the slowest slopes, problems with voltage overshoots and high-frequency oscillations decrease, and, in consequence, the 3LFC variant becomes closer to 2LSC and 2LFC. On the other hand, the distance between the best case and 2LMV rises.

V. DISCUSSION AND COMPARISON

In this section, all four approaches are analyzed and compared using different factors starting from the converter layout through gate driver issues to the system cost, based on the performed tests, as well as on insights from referenced papers. Summary of this considerations is shown in Table 3. Note that this comparison is performed for a 1.5 kV DC system with 450 A modules, and not all conclusions may be suitable for other current/voltage ratings.

A. QUALITY OF WAVEFORMS AT THE INPUT/OUTPUT

Three out of four systems are two-level, while the 3LFC delivers regular three-level voltage to the phase output. For the same switched power and frequency, the content of high-frequency components in output voltage with this variant is lowest, and current ripples are also less severe than in the other approaches. The other three options show the same performance, waveforms in Fig. 5a prove that a short middle state in the 2LFC case makes very little difference. Similar observation can be done in terms of EMC performance: a common-mode noise is less severe for the three-level converter and 2LFC (due to middle states dv/dt is comparable to 3LFC). All in all, a classic multilevel approach seems to be preferable from this point of view.

B. POWER LAYOUT–PARASITIC INDUCTANCES

In terms of power circuit simplicity 2LMV approach is the most convenient, the parasitic inductance and switching conditions are as good as the module packaging [35], [36] and busbar design [28]. As recent SiC MOSFET modules are improved compared to previous versions and the layout of this half-bridge is not challenging, the results in Fig. 3b prove low inductance. At the moment of the paper writing, it was not possible to find a commercial module with series-connected SiC MOSFETs inside. Therefore, the 2LSC option requires two low voltage modules, and the switching loop inductance contains internal inductances of two modules (each of the considered components shows 6.7 nH [34]) and additional connections. But this approach seems advantageous over 2LFC and, especially 3LFC with the large capacitor causing higher inductance and voltage overshoots (Fig. 6b). When the 2LFC approach is discussed, the smaller capacitor is less inductive, and the way of connecting to the circuit is less complex, resulting in better performance.

C. POWER LOSSES

In the considered case of 450 A rated modules, the on-state resistance of 3.3 kV SiC MOSFETs ($r_{DS(ON)} = 5.3$ mΩ) is clearly higher than in 1.2 kV counterparts (2.6 mΩ), but two low-voltage devices are required per switch position. The resistance increase with junction temperature is more visible for MV transistors (87.5% vs. 60% for the rise from 25 °C to 150 °C [33], [34]). Thus, the conduction losses for the same current are slightly lower for low-voltage modules.

The results in Tab. 2 proves that the switching losses are dominant, and the low voltage devices outperform the medium-voltage counterparts. A datasheet-based comparison of switching energy per pulse rated to switched power shows an approximately ten times higher value for MSM450FS33A than for CAB450M12XM3 (802 mJ/kW vs. 78 mJ/kW [33], [34]). In practice, the switching speed of the 3.3 kV module can be increased over datasheet values while low-voltage modules suffer from the voltage overshoots increasing switching energies, and the difference is not as significant. The lowest values of switching losses are observed for series-connected devices, while Q2L operation leads to slightly higher loss. Next are the same modules in three-level operation and the definitely worst case, 2LMV, due to a much slower switching process and significantly higher switching energy.

D. POWER LAYOUT–COOLING

In this aspect, all three solutions with low voltage devices are similar and should be compared together to the 2LMV version. Higher chips size of the medium-voltage power module and a special nHPD2 package offer very low thermal resistance (39 K/kW for MOSFET [33]) – in the case of the low-voltage module, these values are higher (110 K/kW - MOSFET [34]). The heat exchange area is also much higher for MSM450FS33A (140 cm^2 vs. 42.4 cm^2), but this may also impact contact resistance. On the contrary, the power losses are distributed among two smaller power modules (84,8 cm^2 in total), and the heat source is more spread among the heatsink. It is also less challenging to obtain low contact resistance. All in all, it seems that the 2LMV solution is better when cooling is considered, but a higher amount of power loss ends with higher junction temperatures.

E. GATE DRIVERS AND AUXILIARY UNITS

The 2LMV approach with two transistors and standard gate drivers is preferable as the least number of drivers is apparent. On the other hand, four gate drivers are necessary for the other three options, but the crucial disadvantages lie in auxiliary circuits. 3LFC approach always requires an additional voltage balancing system, the same for 2LFC. The worst-case here is the series-connection of the low-voltage devices (2LSC) as a complex control system with fast measurements and high-resolution PWM control must be applied.

F. RELIABILITY AND ROBUSTNESS

Long-term reliability data for new SiC technology is limited, especially for medium voltage devices, which can be more problematic due to higher blocking voltages. Thus, at the moment, it can be predicted that, similarly to Si transistors, devices in 3.3 kV power modules are less reliable than their 1.2 kV counterparts. On the other hand, when the whole system is considered, the number of components in 2LMV is the lowest, while the other three approaches require twice as many transistors and additional auxiliary circuits. The authors believe that two cases 3LFC and 2LFC, would be comparable: 3LFC contains the capacitor operating at high current while 2LFC requires additional circuitry. Again, the system that is the most prone to reliability issues seems to be 2LSC variant as a failure of any component, also in the active balancing system, ends in complete damage of the phase-leg and the time constants to respond to these faults are much shorter compared to 2LFC, and, especially 3LFC, options, as the flying capacitor stores some energy and is capable of enduring faults longer.

G. COST

At this point, the time scale is crucial as medium-voltage SiC technology is delayed and less popular in reference to low-voltage devices available on the market for almost ten years and currently mass-produced. Thus, it is highly likely, that cost factors may change in the future when MV devices also reach higher production volumes, but at the moment, the 1.2 kV modules are around 6-7 times less expensive. Even for two modules necessary in 2LSC, 2LFC, and 3LFC, this factor is unfavorable. On the other hand, 3LFC requires an additional capacitor rated at a high current, while 2LSC and 2LFC need additional measurements and control blocks. However, the cost of these components for the auxiliary circuitry is rather low compared to the medium-voltage power module.

H. START-UP ISSUE

Finally, the last issue is the start-up. Obviously, the 2LMV approach is the simplest as no additional control mechanisms are required, and the systems boots with no issue. When 2LFC and 3LFC methods are considered, there is the need to precharge the flying capacitor or implement special start-up procedures, leading to more complicated control. Lastly, the 2LSC approach also requires addressing this issue, as even when active methods are used, initial voltage conditions may lead to transistor breakage, either in the form of auxiliary circuits or start-up procedures.

VI. CONCLUSION

The comparative study conducted in this paper shows different aspects of MV power switches in SiC technology. While the specific approaches, namely 2LMV, 2LSC, 2LFC and 3LFC, were already presented and analyzed in the literature, a fair comparison with identical operating conditions for all approaches was missing. The conclusions are based on a thorough experimental and multicriterial comparison conducted for four methods, and at such power level (1.5 kV and 300 A). When power losses and system efficiency are key factors, low voltage components are the best choice. In particular, the series-connection of low-voltage transistors shows extraordinary performance, which may be improved with dedicated low-inductive power modules. The additional gain is a low junction temperature and reduced cost, however, the control circuitry is complex. Comparable gains can also be achieved with Q2L operated flying capacitor phase-leg, which in terms of system complexity and reliability is even better than series-connection. This approach is relatively new but seems that it may become popular at medium voltages. But those who can afford system simplicity would definitely prefer a medium-voltage power module. However, in addition to higher cost, an increase in power loss and junction temperature must be taken into account. This approach may look better in a longer time perspective under the assumption that the prices of MV power modules decrease with higher volume. Finally, multilevel solutions, in particular FC topology, may also be attractive for the users familiar with these topologies despite slightly worse switching performance. Last but not least, this approach may also become more favorable when suitable power modules will be available on the market.

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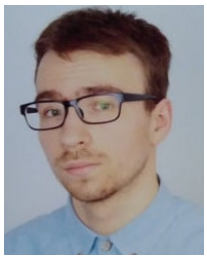

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3.4 Medium voltage flying capacitor dc–dc converter with high-frequency tcm-q2l control [P4]

[P4] **R. Kopacz**, M. Harasimczuk, P. Trochimiuk, G. Wrona and J. Rąbkowski, "Medium Voltage Flying Capacitor DC–DC Converter With High-Frequency TCM-Q2L Control," in IEEE Transactions on Power Electronics, vol. 37, no. 4, pp. 4233-4248, April 2022. Points according to the Ministry of Education and Science: **200**, Impact Factor: **5.967**. Contribution of the dissertation author: **40%**. [129]

Medium Voltage Flying Capacitor DC–DC Converter With High-Frequency TCM-Q2L Control

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***Abstract*—This article presents a novel control method for a multilevel dc–dc flying capacitor converter for applications in medium voltage range. Quasi-two-level modulation provides the possibility to obtain low flying capacitance even below 1 μF, whereas the triangular current mode controller part enables to achieve zero voltage switching at turn-ON for a wide operating range, lowering power losses, and providing the possibility to operate at higher frequencies. The proposed novel control converges the advantages of these both methods leading to very high efficiency with high power density. Performance of the flying capacitor converter with the proposed control method is illustrated with a model-based Saber simulation at first, and then, an experimental model operating at wide frequency range (40 ÷ 250 kHz) and in medium voltage range was designed and constructed. A series of laboratory tests at up to 1.5 kV dc and 10 kW confirmed the noteworthy characteristics of the converter. The voltage between the power devices is balanced and the efficiency achieved reached as high as 99.1%. Therefore, the proposed converter can be competitively employed against classical two-level, as well as three-level and series connection-based counterparts.**

***Index Terms*—Dc–dc power conversion, power converter, power electronics, power MOSFETs, silicon compounds, voltage control.**

I. Introduction

In THE recent years, the environmental requirements to limit the fossil fuel usage and its consequences demand worldwide employment of RES and further improvements in the department of electrical energy conversion, especially in terms of efficiency, power density and cost. In order to achieve these prerequisites, extension to MV range for these systems has been suggested as a prominent solution [1], [2] that is intensively studied by researchers and have already been utilized in the industry. The main applications for dc–dc converters in this voltage range include: dc microgrids for future energy distribution systems as well as for EV charging stations [3]; auxiliary traction converters; and, finally, PV applications [4], [5], which have also adopted 1.5 kV dc voltage rating [6]. Furthermore, some applications in the MV range may additionally require the possibility to convert the energy bidirectionally, such as in ESS, which are vastly used nearly in every type of microgrids. Therefore, there is a great need to provide highly-efficient and low-cost dc–dc converters within the MV level so that all the advantages of this voltage range could be fully utilized.

The main challenge in terms of low-loss MV dc–dc converter construction and design is nested within the core component of each power electronics system, the power switch. In the low voltage area SiC power devices, in particular SiC MOSFETs [7], have already been successfully adopted as they are characterized by superior performance in comparison to standard Si counterparts, especially in regard to high switching speed and low power loss [8], [9]. However, when MV range is considered the blocking voltage of SiC power transistors, even if notably higher than its Si MOSFET equivalents, still is not sufficient for direct application in MV converters, as the widely used Si IGBTs that can reach as high as 6.5 kV. This is an issue, as even though power semiconductor devices with blocking voltages at 10 kV have been presented, their use is still restrained due to complications in regard to driving circuitry, reliability, and very high cost [10]. Moreover, alas, the commonly-available SiC MOSFETs are still limited to just 1.2–1.7 kV. Hence, in order to apply the vast benefits of SiC power devices in MV power converters more sophisticated approach to power switch utilization has to be employed. One method to achieve this is to use multilevel topologies, which in general provides low device voltage stress, low harmonic, and high power capability [11], [12]. Nevertheless, another classic approach in the form of series connection of power devices is very well known as well and, in general, provides superior efficiency and lower cost with limited number of elements [13]. However, since voltage imbalances among the series connected power devices occur, mainly due to mismatches in device parameters and driving circuits [14], in order to operate properly, the final systems require further attention in the form of supplementary voltage balancing circuits, such as passive snubbers [15], or active driving methods [16], [17], which lead to enlarged cost and complexity of the system [18], diminishing some of the advantages in comparison to multilevel topologies. Thus, so that the combination of the best features of these two approaches can be utilized, Q2L approach, presented in [19]–[22], is considered beneficial as it provides the possibility to execute series connection using basic multilevel

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TABLE I
LIST OF ABBREVIATIONS AND SYMBOLS

Symbol	Description	Symbol	Description
2L	two-level	$P_{(L,TL,TH)}$	power loss (*inductor, low switch, high switch*)
3L	three-level	$P_{SW\_OFF(TH)}$	top switch turn-off switching power loss
B1, B2	two-level converter states	PI	proportional-integral
CCM	continuous current mode	PV	photovoltaic
CRM	critical current mode	RES	renewable energy sources
C_F	flying capacitance	R	output resistance
C_H	high voltage-side capacitance	$R_{DC(L)}$	inductor DC resistance
C_L	low voltage-side capacitance	$R_{DS(on)}$	transistor on-resistance
C_{OSS}	MOSFET output capacitance	S, $\overline{S}$	transistor control signals (non-inverted, inverted)
D	duty cycle	t_0 - t_6	time intervals
d_L, d_H	inductor current rising ratio for conventional 3L converter (d_L for voltage gain < 0.5, d_H for voltage gain > 0.5)	t_{Bi}, t_{Fi}, t_{DTi}	length of states Bi, Fi, DTj (i = 1, 2; j = 1,…,4)
		TCM	triangular current mode
D_{LVL}	level ratio	T_{H1}, T_{H2}	high-side transistors
DSP	digital signal processor	T_{L1}, T_{L2}	low-side transistors
DTi	transition converter states (i = 1,…,4)	T_S	switching period
		Q2L	quasi-2-level
ESS	energy storage systems	V_d	datasheet MOSFET turn-off energy test voltage
E_{OFF}	MOSFET turn-off energy	v_{DS}	MOSFET drain-source voltage
EV	electric vehicle	V_{DS_max}	maximum drain-source voltage
F1, F2	three-level converter states	V_{FC}	flying capacitor voltage
FC	flying capacitor	v_{GS}	MOSFET gate-source voltage
FCC	flying capacitor converter	v_{IND}	inductor voltage
f_S	switching frequency	V_H	high voltage-side voltage
f_r	resonant frequency	V_L	low voltage-side voltage
$f_{\Delta iL}$	inductor ripple frequency	v_M	converter leg output voltage
G_V	voltage gain	Z	resonant impedance
I_d	datasheet MOSFET turn-off energy test current	ZCS	zero current switching
		ZVS	zero voltage switching
$I_{FC(disch.)}$	flying capacitor discharge current	Δi_L	inductor current ripple
i_L	inductor current	ΔV_{FC}	flying capacitor voltage ripple
I_{MAX}	maximum inductor current	η	converter efficiency
I_{MIN}	minimum inductor current (absolute)	ω_r	angular frequency of the resonant circuit
I_O	load current	**SUBSCRIPTS**	
L	inductor inductance	(A)	subscript for mode A (voltage gain ≥ 0.5)
MV	medium voltage	(B)	subscript for mode B (voltage gain ≤ 0.5)
P_{conv}	converter power	(THi, TLi)	subscript for transistors (i = 1, 2)
$P_{C(L, TL, TH)}$	conduction power loss (*inductor, low switch, high switch*)		
$P_{core(L)}$	inductor core power loss		

topology—by employing a significantly reduced flying capacitor for minimal amounts of time, just to balance the voltages between the devices. Hence, series-connection-like performance can be reached, using a simple control system and well-known topology with only one additional component.

Since dc–dc converters have been widely used for many years a large variety of topologies and approaches have been presented in the literature [23], also specifically in regard to bidirectional systems [24]. When nonisolated topologies are considered, which are the most common in RES and ES systems, applied in MV range, multilevel [25]–[27], switched capacitor [28], and interleaved [29], [30] systems appear to be one of the most common solutions since they are characterized by high blocking voltage and high power capabilities along with limited power losses. Furthermore, since efficiency is key, especially for higher power systems, approaches utilizing ZVS or ZCS are also often considered as in [31]. However, such converters usually require supplementary circuits, resulting in higher component count, or more advanced control patterns. Furthermore, resonance-based converter topologies are often bound to one operating point, thus, noteworthy efficiencies cannot be reached for wide load range and/or transformation ratios.

In this article, a novel TCM-Q2L control method for a well-known three-level FCC [32]–[34] is proposed. It is based on the convergence of Q2L approach [19]–[22], and TCM [35]–[38] providing the possibility to achieve ZVS at turn-ON for all power transistors without any auxiliary circuits. The converter with the proposed control pattern can be competitively employed in MV range in comparison to other approaches. In particular, when compared with standard two-level dc–dc converters lower stresses are achievable and lower-rated power devices may be applied (1.2 kV SiC MOSFETs for 1.5 kV voltage in this case). Moreover, in contrast to standard approach to series connection the need to employ supplementary voltage compensation methods is omitted, as the balancing is guaranteed with the use of the flying capacitor. Finally, when comparison with classic three-level dc–dc topologies is considered, the converter with the proposed control method is identified by significantly lower volume of the flying capacitor due to the Q2L modulation and higher possible frequencies through the use of the TCM control. Moreover, when high-power systems are considered, the efficiency of the proposed system can reach or even surpass conventional 3L and 2L systems and is comparable both in terms of efficiency and power density with 3L-operated TCM-based converters Furthermore, the proposed converter is capable of operation in a wide load and voltage gain range.

The rest of this article is organized as follows. A list of abbreviations and symbols used is shown in Table I. After a brief introduction showcasing other solutions for dc–dc converters in MV range, in Section II, operation principles of the converter are shown and described, including basic FCC operation, flying capacitor voltage balancing and, finally, Q2L and TCM control description and synthesis. Furthermore, in Section III, simulation study of the converter is shown. Design and practical issues of constructing a prototype model of the proposed converter are shown in Section IV, whereas the experimental validation of the noteworthy characteristics of the proposed system are presented in Section V. A comparison is given in Section VI. Finally, Section VII concludes this article. It is confirmed that the proposed TCM-Q2L control method for a 3L FCC provides a possibility to construct highly efficient dc–dc converters with low passive component volume that is comparable or even surpasses conventional and state-of-the-art solutions in this power/voltage range in terms of performance. This article is an extension of

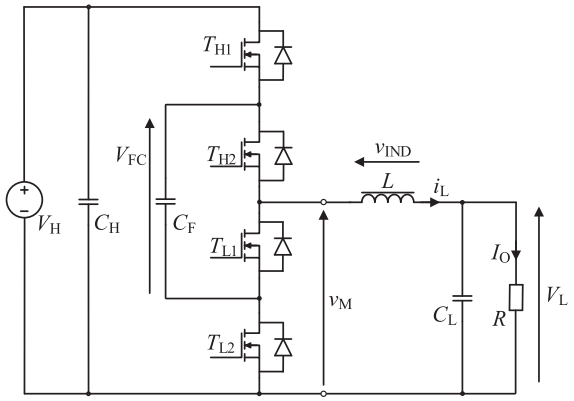

Fig. 1. Scheme of a three-level dc–dc FCC in buck mode

TABLE II
TRANSISTOR SWITCHING STATES OF A 3L DC–DC FCC IN BUCK MODE

State	T_{H1}	T_{H2}	T_{L1}	T_{L2}	v_M	Status
Basic two-level (2L) switching states						
B1	1	1	0	0	V_H	Energy transferred from V_H
B2	0	0	1	1	0	Output charged from L
Basic three-level (3L) switching states						
F1	1	0	1	0	V_{FC}	Charging of the FC
F2	0	1	0	1	V_{FC}	Discharging of the FC
Supplementary switching states						
DT1	1	0	0	0	*var*	Transition between B1/F1
DT2	0	1	0	0	*var*	Transition between B1/F2
DT3	0	0	1	0	*var*	Transition between B2/F1
DT4	0	0	0	1	*var*	Transition between B2/F2

preliminary work described in [39], where a glimpse of the idea was initially presented, but without a thorough theoretical analysis, including optimal, minimal required inductor current to achieve soft switching, and a comprehensive experimental study at rated system voltage, as well as with no comparison to other topologies.

II. TCM-Q2L CONTROL FOR DC–DC FCC

A. Basic FCC Operation Principles

The topology is a classic three-level flying capacitor leg applied in a direct dc–dc converter, as shown in Fig. 1. The converter can operate bidirectionally with the proposed control method. However, for the sake of simplicity, in this article, only buck mode is considered in regard to the theoretical analysis, as well as to the experimental verification.

The switching states of the converter are presented in Table II. States B1 and B2 are used in regard to 2L operation in which the inductor voltage drop is the same as in a classic 2L buck converter, whereas states F1 and F2 correspond to the 3L states employing the flying capacitor. Furthermore, supplementary switching states DT1 to DT4 can be also employed as transitions in-between other converter states. Evidently, in order to use the 3L states as intended, the voltage at the flying capacitance V_{FC} has to be kept constant and equal to $V_{\mathrm{H}}/2$. Therefore, special measures to balance the voltage have to be applied, which will be elaborated on further in the article. The inductor voltage in supplementary states is variable, depending on current circuit state, and equal to either V_{H}, V_{FC} or 0.

B. TCM-Q2L Operation

In a conventional approach to dc–dc FCC control the 3L states F1 and F2 (see Table II) are employed for a considerable amount of time in order to provide the third level of the v_{M} voltage and reduce *di/dt* stress of the inductor. Thus, the required capacitance and, in consequence, the total volume of the flying capacitor have to be relatively high. Using the converter with Q2L control these states are mainly used so that the voltages across the transistor pairs ($T_{\mathrm{H1}}/T_{\mathrm{H2}}$ and $T_{\mathrm{L1}}/T_{\mathrm{L2}}$) can be balanced through the flying capacitor. Therefore, since the 3L times are much shorter, resulting in shorter spans of time in which the capacitor C_{F} conveys the current, the capacitance and its current stress can be substantially reduced in comparison to the standard 3L approach.

In order to describe the Q2L operation more clearly level ratio D_{LVL} describing the relation between the 2L and 3L operation is introduced as in (1), where t_{B1} and t_{B2} are the times of the basic two-level states B1 and B2 shown in Table II and T_{S} is the switching period (transition DT states are omitted)

$$D_{\mathrm{LVL}} = \frac{t_{B1} + t_{B2}}{T_S}. \tag{1}$$

For Q2L mode, since the 3L states are only used for a brief amount of the whole cycle, just to sustain constant voltage equal to $V_{\mathrm{H}}/2$ on the flying capacitor, the ratio D_{LVL} is close to unity (in the prototype $D_{\mathrm{LVL}} > 0.99$), which will be elaborated on further in the article.

When we consider the most basic approach the Q2L modulation pattern only employs the switching states (B1, B2, F1, and F2). However, in an actual real-life system, in which switching time delays have to be considered, the inclusion of supplementary transition states (DT1-4) in order to protect the transistors from short-circuiting via the flying capacitor is necessary. Each of the DT states represents a situation in which only one transistor is turned-ON at a time and it is required, for safety measures, to apply the corresponding DT state in between every state change. Normally, the length of these states T_{DT} is set arbitrarily at a constant value so that safe switching conditions are acquired. However, when MOSFETs are employed as the power devices, carefully choosing the minimum time of these states can be further employed in order to assure ZVS at turn-ON for all the transistors by proper manipulation of the length of the converter states and the switching frequency. In order to achieve ZVS at turn-ON for all voltage gains, the control method is described for both $G_{\mathrm{V}} \geq 0.5$ (mode A) and $G_{\mathrm{V}} \leq 0.5$ (mode B), where G_{V} is the voltage gain of the converter ($G_{\mathrm{V}} = V_{\mathrm{L}} / V_{\mathrm{H}}$), as the current values at which the switching processes occur are different for each mode. Moreover, since DT states, depending on the circuit state, can be used to employ the flying capacitor and balance the voltage among the transistor pairs, in the theoretical analysis the use of states F can be omitted in an ideal case ($D_{\mathrm{LVL}} = 1$).

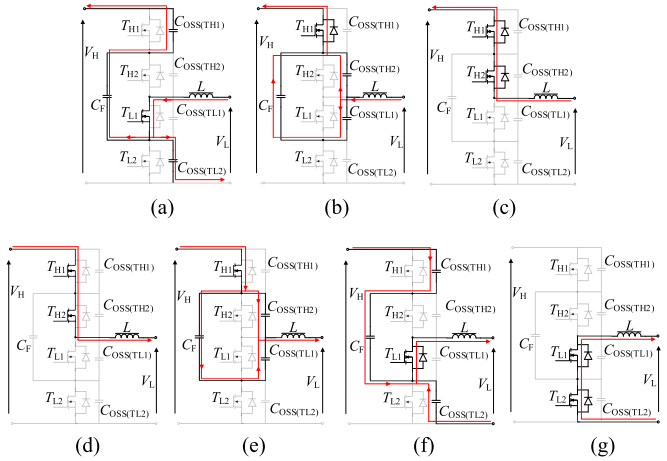

Fig. 2. Operation modes of the converter during exemplary intervals in mode A ($G_V \geq 0.5$). (a) State DT3 with negative inductor current. (b) State DT1 with negative inductor current. (c) State B1 with negative current. (d) State B1 with positive inductor current. (e) State DT1 with positive inductor current. (f) State DT3 with positive inductor current. (g) State B2 with positive inductor current.

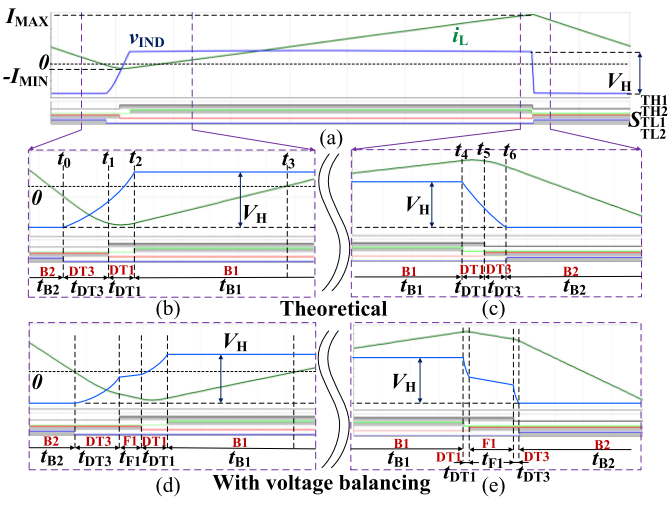

Fig. 3. Proposed modulation pattern for the TCM-Q2L control along with the inductor current and voltage– half of the whole pattern shown as an example for mode A ($G_V \geq 0.5$). (a) One switching period, (b) theoretical pattern for low current transition (c) and high current transition, and the pattern with added three-level states for flying capacitor voltage balancing purposes – (d) low current transition and (e) high current transition.

To explain the idea of TCM in this converter transistor switching states and an exemplary modulation pattern of one of the two sequences with the proposed control method converging TCM and Q2L and focusing on transition between states B2 – F1 – B1 will be considered - see Figs. 2 and 3 for mode A ($G_V \geq 0.5$) and Figs. 4 and 5 for mode B ($G_V \leq 0.5$). In these figures two of the zoomed patterns [see Figs. 3(b), (c) and 5(b), (c)] are shown for theoretical analysis ($D_{LVL} = 1$), whereas the other two [see Figs. 3(d) and (e) and 5(d) and (e)] are presented in regard to a situation in which additional F states are used for flying capacitor voltage balancing ($D_{LVL} = 0.975$). For visibility reasons, the ratio between two-level and three-level states D_{LVL} in this figures is lowered and during actual operation three-level states are much shorter.

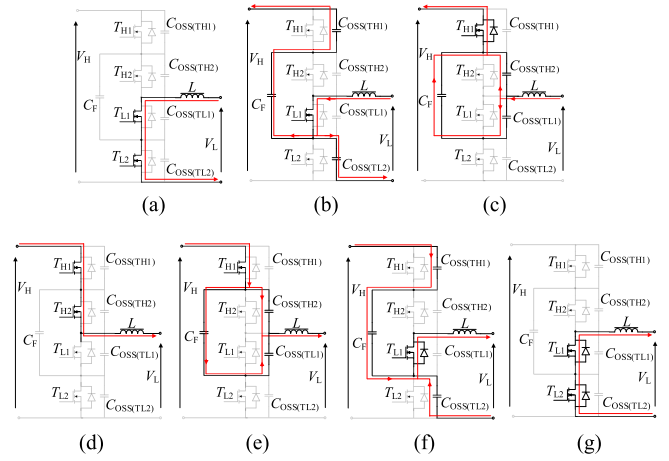

Fig. 4. Operation modes of the converter during exemplary intervals in mode B ($G_V \leq 0.5$). (a) State B2 with negative inductor current. (b) State DT3 with negative inductor current. (c) State DT1 with negative inductor current. (d) State B1 with positive inductor current. (e) State DT1 with positive inductor current. (f) State DT3 with positive inductor current. (g) State B2 with positive inductor current.

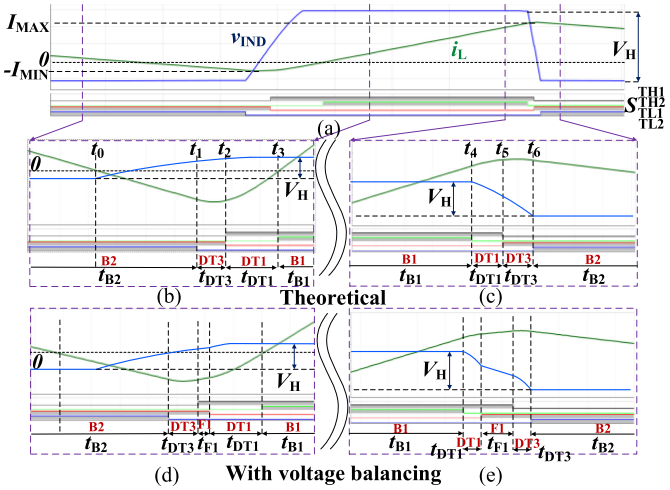

Fig. 5. Proposed modulation pattern for the TCM-Q2L control along with the inductor current and voltage – half of the whole pattern shown as an example for mode B ($G_V \leq 0.5$). (a) One switching period, (b) theoretical pattern for low current transition (c) and high current transition, and the pattern with added three-level states for flying capacitor voltage balancing purposes – (d) low current transition and (e) high current transition.

In order to simplify the circuit analysis constant voltage equal to half of the input voltage on output and flying capacitor during one switching period is assumed. Voltage drop on conducting diodes and transistors, as well as parasitic parameters, except for transistor output capacitances as these are crucial in order to explain the soft-switching mechanism in the proposed converter, of all components, as well as the turning time of switches, are omitted. Furthermore, transistor output capacitances C_{OSS} are assumed constant and equal for all the switches.

The thought process for all the equations for all the intervals is as follows: the system consists of a resonance circuit containing the inductor L and two parallel-connected transistor output capacitances $2C_{OSS}$ (e.g., $C_{OSS(TH1)}$ and $C_{OSS(TL2)}$, where

$C_{\mathrm{OSS(TH1)}} = C_{\mathrm{OSS(TL2)}} = C_{\mathrm{OSS}}$). Thus, resonance impedance Z and resonance angular frequency ω_{r} can be described as follows:

$$Z = \sqrt{\frac{L}{2C_{\mathrm{OSS}}}} \tag{2}$$

$$\omega_r = \frac{1}{\sqrt{2LC_{\mathrm{OSS}}}}. \tag{3}$$

The said resonant circuit is supplied by the main capacitors of the system C_{H}, C_{L}, C_{F}, which are assumed to have constant voltage and are equal to, subsequently, V_{H}, V_{L}, V_{FC}. Thus, an equivalent circuit, consisting of inductance L, capacitance $2C_{\mathrm{OSS}}$ and, depending on the specific interval, a combination of capacitances modelled as constant voltage sources (V_{H}, V_{L}, V_{FC}), can be derived and then used to describe the inductor current, and the duration of a specific interval as shown further in the Section.

Interval 1 (t 0 – t 1) Figs. 2(a), 3(b) *(mode A);* 4(a), 5(b) *(mode B):*

In the time before the considered interval transistors T_{L1} and T_{L2} are turned ON and conduct, whereas transistors T_{H1} and T_{H2} are turned OFF. At time t_0 inductor current i_L is equal to 0.

In mode A, at time t_0 transistor T_{L2} is turned-OFF and the resonant operation starts between inductor L and output capacitances $C_{\mathrm{OSS(TH1)}}$ and $C_{\mathrm{OSS(TL2)}}$. During this interval capacitance $C_{\mathrm{OSS(TH1)}}$ is discharging and capacitance $C_{\mathrm{OSS(TL2)}}$ is charging. Inductor current in the considered interval can be described by the following equation:

$$i_{L(A)}(t) = \frac{-V_L}{Z}\sin(\omega_r t). \tag{4}$$

In mode A, the interval ends when capacitance $C_{\mathrm{OSS(TH1)}}$ is fully discharged, which allows to turn-ON transistor T_{H1} at zero voltage. On the basis of (4) the duration of the interval can be calculated

$$t_{1(A)} - t_0 = \cos^{-1}\left(\frac{G_V - 1/2}{G_V}\right)\frac{1}{\omega_r}. \tag{5}$$

Unlike in mode A, in mode B transistor T_{L2} is turned-OFF at current lower than zero. Thus, for this mode, the interval starts when inductor current i_{L} reaches 0, while both T_{L1} and T_{L2} are still ON. Inductor L current is this interval is given by

$$i_{L(B)}(t) = -V_L \cdot t/L. \tag{6}$$

The length of the considered interval in mode B can be computed as

$$t_{1(B)} - t_0 = -\frac{i_L(t_{1(B)}) \cdot L}{V_L}. \tag{7}$$

Interval 2; (t 1 – t2), Figs. 2(b), 3(b) *(mode A);* 4(b), 5(b) *(mode B):*

At the beginning of the interval in mode A transistor T_{H1} is turning ON at zero voltage and transistor T_{L1} is turning OFF, which enables resonant operation between inductor L and transistor output capacitances $C_{\mathrm{OSS(TH2)}}$ and $C_{\mathrm{OSS(TL1)}}$. The interval ends when capacitance $C_{\mathrm{OSS(TH2)}}$ is fully discharged and can be described by following equations:

$$i_{L(A)}(t) = \frac{-V_L}{Z}\sin\left\{\omega_r\left[t + (t_{1(A)})\right]\right\} \tag{8}$$

$$t_{2(A)} - t_{1(A)} = \cos^{-1}\left(\frac{G_V - 1}{G_V}\right)\frac{1}{\omega_r}. \tag{9}$$

At the end of the interval in mode A, transistor T_{H2} is turned ON at zero voltage.

In mode B, on the other hand, transistor T_{L2} is turned OFF at the start of the interval, which initiates resonant operation between inductor L and output capacitances $C_{\mathrm{OSS(TH1)}}$ and $C_{\mathrm{OSS(TL2)}}$. The interval ends when capacitance $C_{\mathrm{OSS(TH2)}}$ is fully discharged and can be described by following equations:

$$i_{L(B)}(t) = \frac{-V_L}{Z}\sin\left\{\omega_r(t) + \sin^{-1}\left[-i_L(t_{1(B)} - t_0)\right]\right\} \tag{10}$$

$$t_{2(B)} - t_{1(B)} = \cos^{-1}\left(\frac{G_V}{G_V - 1}\right)\frac{1}{\omega_r}. \tag{11}$$

Interval 3 (t 2 – t 3) Figs. 2(c), 3(b) *(mode A);* 2(c), 5(b) *(mode B):*

In mode A, the interval starts when transistor T_{H2} is turning ON at zero voltage. Current in inductor L rises linearly in accordance to the following equations:

$$i_{L(A)}(t) = i_L(t_{2(A)}) + (V_H - V_L) \cdot t/L. \tag{12}$$

The interval ends when inductor current is equal to zero and the length of this interval can be given by

$$t_{3(A)} - t_{2(A)} = -\frac{i_L(t_{2(A)}) \cdot L}{V_H - V_L}. \tag{13}$$

In mode B, the interval begins when transistor T_{L1} is turning OFF, transistor T_{H1} turns-ON at zero voltage and inductor L and capacitances $C_{\mathrm{OSS(TH2)}}$, $C_{\mathrm{OSS(TL1)}}$ resonate. Inductor L current is given by

$$i_{L(B)}(t) = \frac{-V_L}{Z}\sin\left\{\omega_r(t) + \sin^{-1}\left[i_L(t_{2(B)})\right]\right\}. \tag{14}$$

The considered interval length is given by the following equation:

$$t_{3(B)} - t_{2(B)} = \cos^{-1}\left(\frac{1/2 - G_V}{1 - G_V}\right)\frac{1}{\omega_r}. \tag{15}$$

Interval 4; (*t 3 – t 4*), Figs. 2(d), 3(c) *(mode A);* 4(d), 5(c) *(mode B):*

During this interval high side transistors T_{H1} and T_{H2} remain ON, low side transistors T_{L1} and T_{L2} remain OFF. The energy from input voltage source V_{H} is transferred to the inductor L and load consisting the parallel connection of output resistance R and output capacitor C_{L}. Inductor current i_{L} rising linearly and can be described by the following equation:

$$i_L(t) = \frac{V_H - V_L}{L}t. \tag{16}$$

Interval 5; (*t 4 - t 5*); Figs. 2(e), 3(c) *(mode A);* 4(e), 5(c) *(mode B):*

At the beginning of the interval transistor T_{H2} is turned OFF. Capacitance $C_{\mathrm{OSS(TH2)}}$ is charging and capacitance $C_{\mathrm{OSS(TL1)}}$

is discharging. Assuming that inductor current is constant in the considered interval, its length can be described by

$$t_5 - t_4 = \frac{V_H C_{\mathrm{OSS}}}{i_L(t_4)}. \tag{17}$$

Interval 6; (t 5 - t 6); Figs. 2(f), 3(c) *(mode A);* 4(f), 5(c) *(mode B):*

At the beginning of the interval transistor T_{L1} is turning ON at zero voltage and transistor T_{H1} is turning OFF. Capacitance $C_{\mathrm{OSS(TH1)}}$ is charging and capacitance $C_{\mathrm{OSS(TL2)}}$ is discharging. When constant inductor current is assumed in the interval, the length is calculated by

$$t_6 - t_5 = \frac{V_H C_{\mathrm{OSS}}}{i_L(t_5)}. \tag{18}$$

Interval 7; (t 6 - t 0); Figs. 2(g), 3(c) *(mode A);* 4(g), 5(c) *(mode B):*

At the start of the considered interval transistor T_{L2} is turning ON at zero voltage. Energy accumulated in the inductor is transferred to the load. Inductor current i_{L} reduces linearly and can be described by the following equation:

$$i_L(t) = i_L(t_6) - \frac{V_L}{L}t. \tag{19}$$

Thus, one switching sequence is concluded. However, in order to maintain the natural flying capacitor voltage balancing, which is elaborated on further in the article, the full modulation sequence includes other transitions, in which the soft switching conditions are analogous to these shown in Figs. 3 and 5. Therefore ZVS at turn-ON for all the transistors is achieved. Moreover, since DT intervals are very short, their impact on the inductor current can be omitted, and, in consequence, on the output voltage as well. However, DT states are still crucial for achieving proper voltage on the flying capacitor.

C. Voltage Gain and Switching Frequency

In the proposed converter, the control parameters, such as switching frequency and duty cycle, are determined by voltage gain G_{V} and output resistance R according to the principle operation described by (4)–(19). Furthermore, switching frequency and duty cycle differ based on the voltage gain—mode A ($G_{\mathrm{v}} \geq 0.5$) and mode B ($G_{\mathrm{v}} \leq 0.5$)—and can be calculated based on the following equations, where D ($D_{(\mathrm{A})}$ for mode A and $D_{(\mathrm{B})}$ for mode B) is the duty of the converter defined as the ratio between the time in which the converter operates in state B1 (T_{H1} and T_{H2} are ON) and the switching period T_{S}

$$G_{V(A)} = -\frac{RD_{(A)}{}^2}{4f_sL} + \sqrt{\left(\frac{RD_{(A)}{}^2}{4f_sL}+1\right)^2 - \frac{RD_{(A)}\sqrt{2G_V-1}}{Z}} - 1 \tag{20}$$

$$D_{(A)} = G_{V(A)}\left(\frac{1}{2\pi}\left[\cos^{-1}\left\{\frac{1-G_{V(A)}}{G_{V(A)}}\right\} - \pi\right]\frac{f_s}{f_r} + 1\right) \tag{21}$$

$$G_{V(B)} = \frac{RD_{(B)}{}^2}{4f_sL}\left(\sqrt{\frac{8f_sL}{RD_{(B)}{}^2}+1} - 1\right) \tag{22}$$

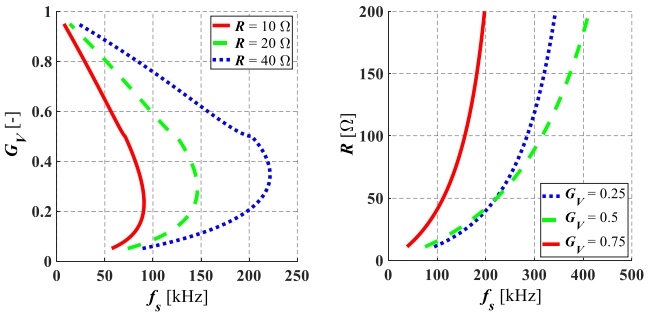

Fig. 6. Control characteristics – frequency dependence on (a) voltage gain and (b) load parameters for the parameters of the prototype.

$$D_{(B)} = G_{V(B)}\left(1 - \frac{1}{2\pi}\cos^{-1}\left[\frac{G_{V(B)}}{G_{V(B)}-1}\right]\frac{f_s}{f_r}\right) - \frac{f_sL\sqrt{1-2G_{V(B)}}}{Z}. \tag{23}$$

Voltage gain G_{V} and duty cycle D were determined on the basis of (2)–(19). To achieve soft switching, converter should operate with a specific frequency and particular duty cycle depending directly on load resistance R and voltage gain G_{V}. According to the analysis, for certain R and G_{V} there is one, specific frequency that ensures optimal conditions so that ZVS can be achieved.The control characteristics plotted for the converter on the basis of the presented formulas are shown in Fig. 6. The transformation ratio dependence on frequency for various load resistance is displayed in Fig. 6(a), whereas Fig. 6(b) presents the load resistance in function of the switching frequency for a few voltage gains G_{V}.

D. Soft Switching Conditions

In the proposed converter to achieve zero-voltage at turn-ON for all the transistors, these have to switch at certain conditions. Each transistor turn-ON process must be initiated when its output capacitance has already been discharged, which is assured through providing specific length of the DT states and with certain minimal inductor current at which the turn-ON process will occur according to equations in the previous section. This is realized via variable frequency control depending on the load parameters and the voltage gain.

To be more specific, soft turning-ON of transistors T_{H1} and T_{H2} require to turn-ON T_{L1} and T_{L2} transistors at certain times in order to provide enough current to discharge capacitances $C_{\mathrm{OSS(TH1,\ TH2)}}$. Formulas for the specific times are presented in Section II-B. In mode A, transistor T_{L2} has to be turned-OFF at the time when the inductor current reaches 0. However, in order to provide full ZVS at turn-ON in mode B ($G_{\mathrm{V}} \leq 0.5$) transistor T_{L2} should be turning OFF at specific current, in accordance with the following equation:

$$i_L(t_{1(B)}) = -\frac{V_H\sqrt{1-2G_V}}{Z}. \tag{24}$$

Capacitances C_{OSS} of transistors T_{L1} and T_{L2} are discharging in intervals 5 and 6, which allows to achieve ZVS at turn-ON similarly as for the high-side transistors T_{H1} and T_{H2}, but since

the inductor current value is much higher, the interval lengths are much shorter and thus it is assumed that the currents for both these transitions are constant throughout the whole DT state and identical for both DT1 and DT3. Moreover, both low-side transistors T_{L1} and T_{L2} are turning-OFF at very low current values (ZCS).

The analysis of the converter operation was carried out with the assumption that the value of current flow from the load to the circuit is minimized. However, since this current is required to enable soft turn-ON for the transistors, it is still apparent. Thus, it is worth noting that when this modulation method is employed the conduction losses rise slightly in comparison to a more common approach with positive inductor current throughout the whole switching cycle (CCM). Thus, low conduction loss power devices should be considered. Nevertheless, the DT time interval should be minimized to just enough to provide the possibility to reach ZVS at turn-ON but not extend this time excessively in order to maximize the efficiency.

Furthermore, even though in order to assure ZVS conditions for the transistors the inductor current i_{L} must reach negative values (near-CRM) the output capacitor C_{L} filters the high-frequency part of the current and, thus, the output voltage is constant and positive and, therefore, the system can be applied in applications such as ESS or fuel cells.

E. Voltage and Current Stress of Semiconductor Power Components

Assuming flying capacitor voltage at $V_{\mathrm{H}}/2$ and omitting oscillations maximum voltages on all transistors are the same for all the devices and equal to

$$V_{DS\_\max(\mathrm{TH1,TH2,TL1,TL2})} = V_H/2. \tag{25}$$

RMS currents were calculated excluding the resonant operation between inductor L and transistors output capacitances C_{OSS} and assuming that $G_V = D$. In that case, rms currents in transistors are given by

$$I_{\mathrm{rms(TH1,TH2)}} = 2I_O\sqrt{G_V/3} \tag{26}$$

$$I_{\mathrm{rms(TL1,TL2)}} = 2I_O\sqrt{(1-G_V)/3}. \tag{27}$$

And the rms inductor current is

$$I_{\mathrm{rms(L)}} = 2I_O/\sqrt{3}. \tag{28}$$

F. Voltage Ripple on the Flying Capacitor

In a basic buck–boost three level converter, as noted in Section II-B, flying capacitor C_{F} conducts through a significant part of the converter cycle, which has a substantial effect on capacitor voltage ripple and, thus, requires using a capacitor with high value of capacitance. In the proposed operation method, flying capacitor is employed only in intervals when output capacitances of transistors are charging/discharging and during transition DT states. Voltage ripple on the flying capacitor can be described based on the following equation (assuming identical output capacitance for all the transistors):

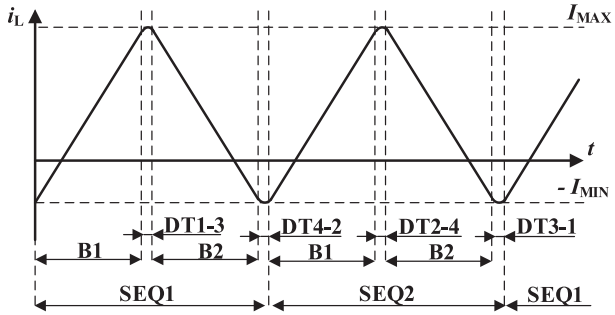

Fig. 7. Sequence order and states for natural flying capacitor balancing.

$$I_{\mathrm{FC(disch.)}} = \frac{\int_{t0}^{t2(A)} i_L(t)dt}{t_{2(A)} - t_0} = \frac{2C_{\mathrm{OSS}}V_H}{t_{2(A)} - t_0} \tag{29}$$

$$\Delta V_{\mathrm{FC}} = \frac{I_{FC(\mathrm{disch.})}(t_{2(A)} - t_0)}{C_F} = \frac{2V_H C_{\mathrm{OSS}}}{C_F}. \tag{30}$$

However, this equation was synthesized for the theoretical modulation pattern employing only states B and DT [see Figs. 3(b) and (c) and 5(b) and (c)]. When actual operation of the converter with additional flying capacitor voltage balancing via states F [see Fig. 3(d), (e) and 5(d), (e)] is considered the ripples may be slightly higher.

G. Flying Capacitor Voltage Balancing

As mentioned before, in order to have the converter operate properly, the voltage on the flying capacitor V_{FC} must be constant and equal to $V_{\mathrm{H}}/2$. There have been many different flying capacitor voltage balancing methods proposed [11], [19]. In general, these can be divided into two main groups: classic active methods employing closed loop control systems, based on either voltage measurement [40] or more sophisticated sensorless approach [33], and suitable alteration in the modulation pattern to ensure stable flying capacitor voltage; and natural balancing methods [41] that generally operate in open loop, which rely on having the average current in the flying capacitor equal to zero during the whole switching cycle. Moreover, it can be noted the model predictive control-based methods can be used with either approach (e.g., active [42] or natural [43]). In this article, the proposed control method includes flying capacitor voltage balancing based on the convergence of conventional voltage measurement-based active and natural balancing, where stability of operation with zero average FC current in steady state is ensured through natural balancing, whereas the robustness in terms of parameter mismatches, such as differences in transistor output capacitances C_{OSS} or delays in the signal paths, is assured through the active controller part.

First OFF, the system operates using two state sequences (31), (32) alternately, as shown in Fig. 7, so that the capacitor gets charged and discharged with the same amount of current within

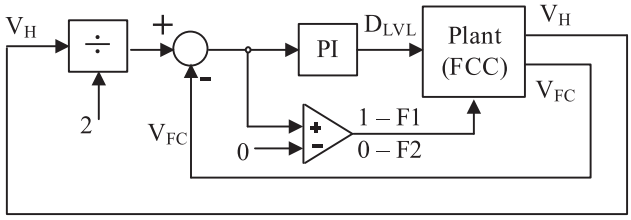

Fig. 8. Block diagram of the flying capacitor voltage balancing control loop.

these two sequences

$$\text{SEQ1} = B1- > DT1- > DT3- > B2- > DT4- > DT2 \tag{31}$$

$$\text{SEQ2} = B1- > DT2- > DT4- > B2- > DT3- > DT1. \tag{32}$$

In order to justify such approach, a situation in which only SEQ1 is used may be showcased as an counterexample. Then, the capacitor would be always discharged (state F2) with high inductor current (I_{MAX}) whereas the charging (state F1) would occur with lower inductor current (I_{MIN}) described by equations from (4) to (15). Therefore, the capacitor would draw less energy than it would receive resulting in an unbalanced voltage below the desired level ($V_{\text{FC}} < V_{\text{H}}/2$). Thus, applying the presented sequence order guarantees (assuming constant inductor current) that the same amount of energy is transferred from and into the flying capacitor and, therefore, will result in natural voltage balancing.

However, when the converter conditions shift, for example due to change in supply voltage or load values, the inductor current fluctuates and the natural balancing sequence will not be sufficient. Therefore, second balancing measure, in form of a closed-loop controller shown in Fig. 8 is applied as well. Based on the measurement of the voltages V_{H} and V_{FC} it is known whether the flying capacitor is balanced at $V_{\text{H}}/2$ and further the error signal can be applied in a PI controller, which regulates the value of D_{LVL}, applying additional intervals and its converter states F1 and F2 according to Table II in-between the transition states, as shown in Figs. 3(d) and (e) and 5(d) and (e). Furthermore, depending whether the flying capacitor voltage is too high or too low, either discharging state F2 or charging state F1 is applied for the amount of time defined by D_{LVL}.

Moreover, as in any FCC, additional, well-known start-up measures are required in order to assure stable FC voltage during system initialization, e.g., using precharging [44].

III. Simulation Study

In order to initially validate the proposed TCM-Q2L control method for a FCC a simulation study in Synopsys Saber was conducted, so that the power MOSFET modeling tool could be employed for semiconductor power transistors ensuing highly accurate results, as simulating the resonance between the output MOSFET capacitances and the inductor requires precise switching models.

Since the converter was to operate at a maximum of 1.5 kV of dc voltage 1.2 kV SiC MOSFETs (FF11MR12W1M1_B11) from Infineon were chosen as the power devices based on preliminary

TABLE III
Parameters of the Converter

Parameter	Description
Max DC voltage	1500 V
Switching frequency	40 ÷ 260 kHz
Voltage gain	0 ÷ 1
SiC power transistors	1.2 kV and 11 mΩ FF11MR12W1M1_B11
Inductor	30 µH/100 A peak
Flying capacitor	330 nF/1000 V
Output/input capacitors	6 µH/1600 V

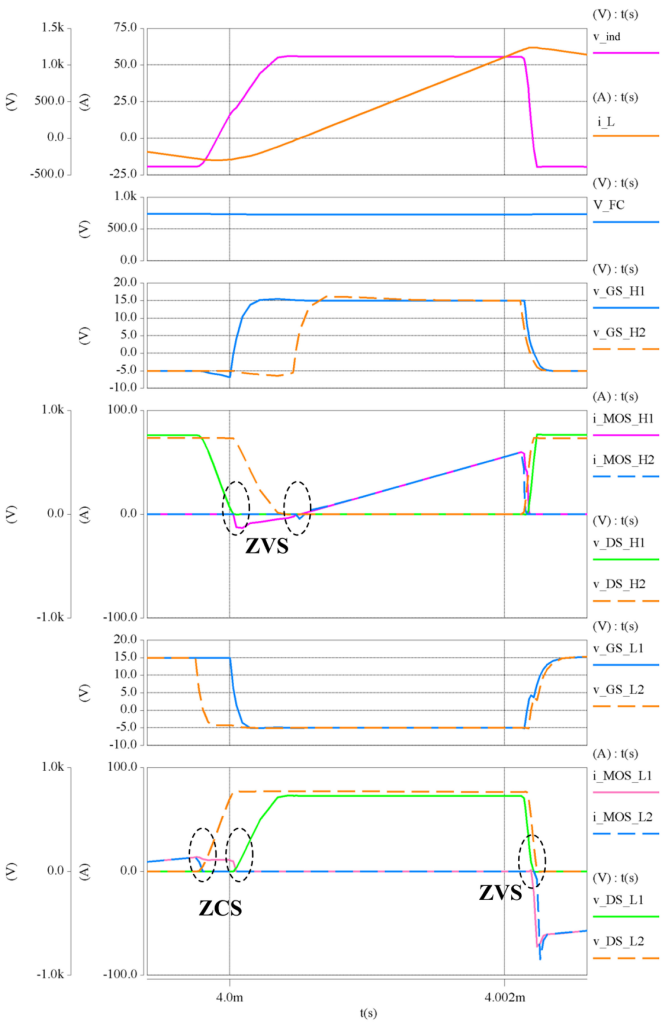

Fig. 9. Exemplary results of the converter operation with the proposed TCM-Q2L control method from the simulation study. Simulation performed at 1500 V dc input voltage, voltage gain G_{V} at 0.2 with a load resistance of 17.2 Ω. From the top: inductor voltage (v_{IND}) and current (i_{L}); flying capacitor voltage (V_{FC}); gate-source voltages of high-side transistors (v_{GSTH1}, v_{GSTH2}); MOSFET currents (i_{MOSTH1}, i_{MOSTH2}) and transistor drain-source voltages (v_{DSTH1}, v_{DSTH2}) of high-side switches; gate-source voltages of low-side transistors (v_{GSTL1}, v_{GSTL2}); MOSFET currents (i_{MOSTL1}, i_{MOSTL2}) and transistor drain-source voltages (v_{DSTL1}, v_{DSTL2}) of low-side switches.

power loss estimations and further selection among the state-of-the-art semiconductors. The parameters of the converter for both simulation and experimental study are shown in Table III.

Fig. 9 shows the results from an exemplary simulation of one of the operating points of the converter—a test performed at 1500 V dc input voltage and voltage gain G_{V} at 0.2 with

a load resistance of 17.2 Ω, in which the switching frequency settled at roughly 121 kHz. The presented results and conducted simulation tests confirm the theoretical presumptions on the converter operation. On the first waveform from the top characteristic shape of the inductor voltage and current can be observed, where voltage v_{IND} resembles classic two-level solution but with extended slopes, whereas current i_{L} is characterized by visible resonant influence near I_{MIN} value. Further on Fig. 9, flying capacitor voltage is showcased to be balanced at 750 V and with minimal ripples, which assures balanced voltage distribution among transistor pairs (v_{DSTH1}, v_{DSTH2} and v_{DSTL1}, v_{DSTL2}), which is also visible on the next waveforms. Moreover, the figure showcases ZVS operation at turn-ON for all the power semiconductor devices through i_{MOS}, v_{DS}, and v_{GS} curves. Furthermore, near-ZCS transition for the turn-OFF process for the low-side transistors can be noted as well.

IV. Laboratory Model

The next step was to design and construct a MV prototype of the FCC with the proposed TCM-Q2L control method based on electro-thermal calculation using the simulation study outcomes and datasheets. The main parameters of the experimental system are identical as in the simulation study and are showcased in Table III. As the converter operates in Q2L mode the flying capacitor C_{F} could be set to only 330 nF in order to achieve voltage ripples ΔV_{FC} below 5% of V_{FC} voltage, which is notably less than in standard multilevel approach. Moreover, in order to sustain manageable voltage ripples at the input and the output of the converter 6 μH/1600 V capacitance was applied for both ends of the system (C_{H} and C_{L}). Furthermore, a 30 μH inductor was used so that roughly 100 kHz operating frequency at 17.2 Ω load resistance and voltage gain G_{V} of 0.5 could be achieved as nominal parameters.

Moreover, since the converter was to operate at notable frequencies even up to 250 kHz and with voltage of 1500 V dc resulting in high *dv/dt* rates, special care was given to the design of the power circuit. The path length of the main power loops and gate connections were minimized so that the parasitic inductances between the switching components could be reduced. The applied isolated gate drivers were self-made based on UCC21750 chip and suggestions from [45], providing suitable protection measures for safe operation of the converter and satisfactory switching performance as 5 Ω gate resistances were used. Furthermore, Fischer LA V 8 with forced air convection was used as the heatsink. The required measurements of voltages V_{H} and V_{F} were delivered using analog circuits based on isolated voltage followers. Finally, the whole system was controlled through a control board, based on floating-point DSP (TMS320F28379D), and mounted on a grounded cover on the side of the converter in order to shield it from the interferences generated by the system. The constructed converter prototype is presented in Fig. 10.

V. Experimental Study

In order to fully validate, the proposed control method for the FCC a series of experimental tests was performed with

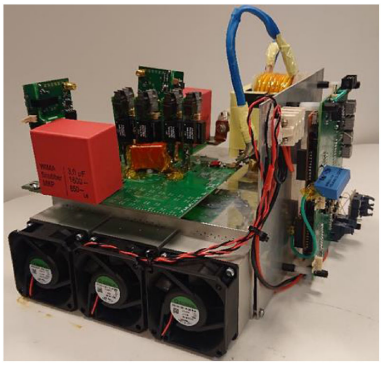

Fig. 10. Photograph of the constructed converter prototype.

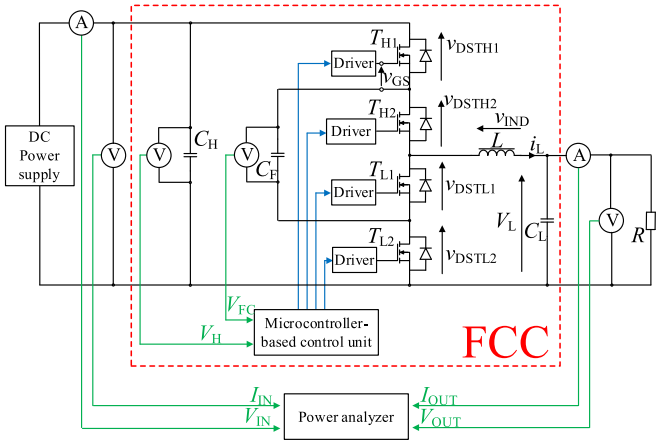

Fig. 11. Scheme of the experimental setup.

up to 1500 V dc voltage and up to 10 kW power with the constructed prototype. The main purpose of this article was to plot experimental characteristics of the TCM-Q2L control method along with the measurements of component stresses and the system efficiency for various loads R and voltage gain G_{V} ratios. The experimental system consisted of the FCC with a resistive load supplied by a dc power supply from Magna-Power. The power and efficiency measurements were performed using Norma LEM 6000 power analyzer, whilst the oscillograms were acquired by Tektronix MSO56 oscilloscope with isolated voltage probes (Tektronix THDP0100 and P2505A) and a current probe (Tektronix TCP303). The scheme of the experimental setup is shown in Fig. 11.

At first, the converter was tested with nominal input voltage of 1500 V and load resistance of 17.2 Ω. Due to limitations in regard to the power supply capabilities (2 kV, 5 A) the power for the experiment was constrained to roughly 5.5 kW with limited voltage gain G_{V} at 0.2 (mode B). Such parameters resulted in the system to operate at 122 kHz switching frequency. The results from this test are showcased in Fig. 12. As shown on the top oscillogram [see Fig. 12(a)] the flying capacitor voltage V_{FC} is balanced with limited ripples below 5% of the nominal voltage equal to 750 V. Furthermore, the inductor voltage v_{IND} has characteristic Q2L-control shape, where the 3L state is employed

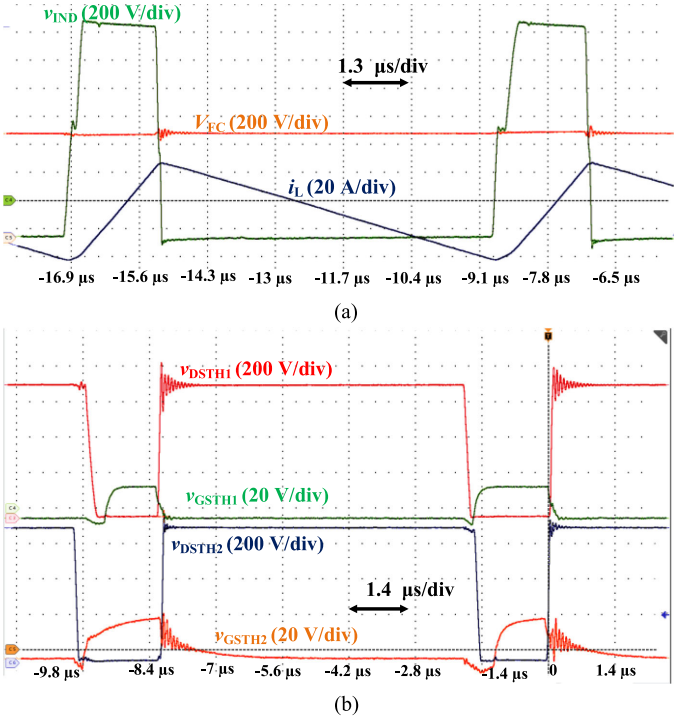

Fig. 12. Experimental results from an experiment performed at 1500 V dc input voltage, mode B (voltage gain G_V at 0.2) with a load resistance of 17.2 Ω - roughly 5.5 kW power at 122 kHz switching frequency – (a) general view and (b) top transistor pair-focused view. From the top: inductor voltage (v_{IND}) and current (i_L); flying capacitor voltage (V_{FC}); gate-source voltages of top-side transistors (v_{GSTH1}, v_{GSTH2}); transistor drain-source voltages (v_{DSTH1}, v_{DSTH2}) of top-side switches.

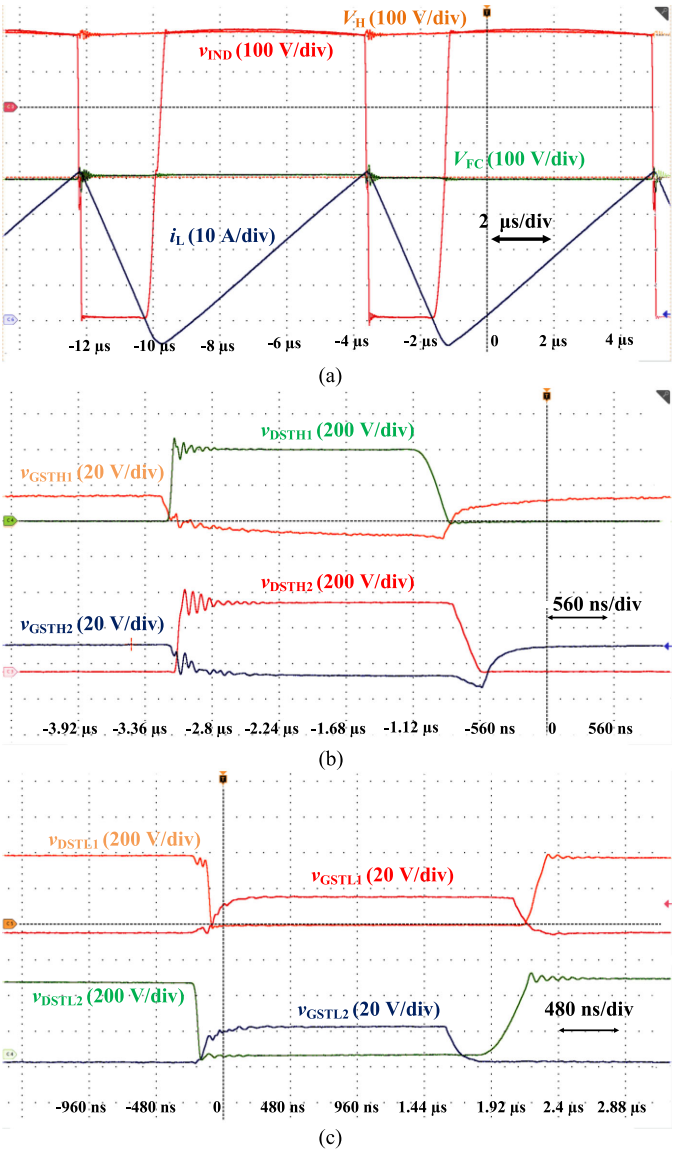

Fig. 13. Experimental results from an experiment performed at 800 V dc input voltage, mode A (voltage gain G_V at 0.7) with a load resistance of 34.6 Ω - roughly 10 kW power at 116 kHz switching frequency– (a) general view, (b) top transistor pair-focused view and (c) low transistor pair-focused view (c). From the top: input voltage (V_H); inductor voltage (v_{IND}) and current (i_L); flying capacitor voltage (V_{FC}); gate-source voltages of top-side transistors (v_{GSTH1}, v_{GSTH2}); transistor drain-source voltages (v_{DSTH1}, v_{DSTH2}) of top-side switches; gate-source voltages of low-side transistors (v_{GSTL1}, v_{GSTL2}); transistor drain-source voltages (v_{DSTL1}, v_{DSTL2}) of low-side switches.

only for a very brief moment (D_{LVL} in this test settled close to 0.995). Inductor current i_L reached roughly 27 A rms value with peak-to-peak current at 70 A. The oscillogram in Fig. 12(b) presents the results from another test with the same parameters. Gate-source voltages are shown next to drain-source voltages in order to showcase ZVS at turn-ON for the devices, and, as the drain-source voltages clearly reach 0 before the gate-source voltage achieve its threshold value, ZVS is confirmed. Moreover, even though voltage oscillations are clearly visible at turn-OFF, the peak drain-source voltage values settled below 900 V, with OFF values equal to V_{FC}, therefore, the transistors operated within safe conditions throughout the whole test.

In order to validate the converter operating at higher power and with higher voltage gain, the rest of the experimental tests were performed using another power supply, also from Magna-Power (800 V, 12.5 A), with capabilities of up to 10 kW. The load resistance R in this tests varied from 10 up to 200 Ω with diverse voltage gains from 0.15 up to 0.75, which resulted in operating frequency of 40 to 250 kHz.

The next Fig. 13 presents results from a test conducted at 800 V dc input voltage, in mode A (voltage gain G_V at 0.7) with a load resistance of 34.6 Ω—resulting in roughly 10 kW power at 116 kHz switching frequency. Similarly as before, the top oscillogram [see Fig. 13(a)] presents balanced V_{FC} voltage, inductor current i_L and voltage v_{IND} and also input voltage V_H, whereas the next two oscillograms in [see Fig. 13(b) and (c)] showcase the switching performance for two transistor pairs (T_{H1}, T_{H2} and T_{L1}, T_{L2}). In this experiment, the inductor current established at 24 A rms and 50 A peak-to-peak values and the flying capacitor voltage ripples settled below 5%. Moreover, ZVS turn-ON transition can be observed for all the devices. Furthermore, near-ZCS turn-OFF for the low-side transistor pair (T_{L1}, T_{L2}) can be observed as well.

Fig. 14(a) showcases results from an experiment performed at 800 V dc input voltage, voltage gain G_V at 0.5 with a load resistance of 34.6 Ω, which lead to 5.2 kW power at 178 kHz

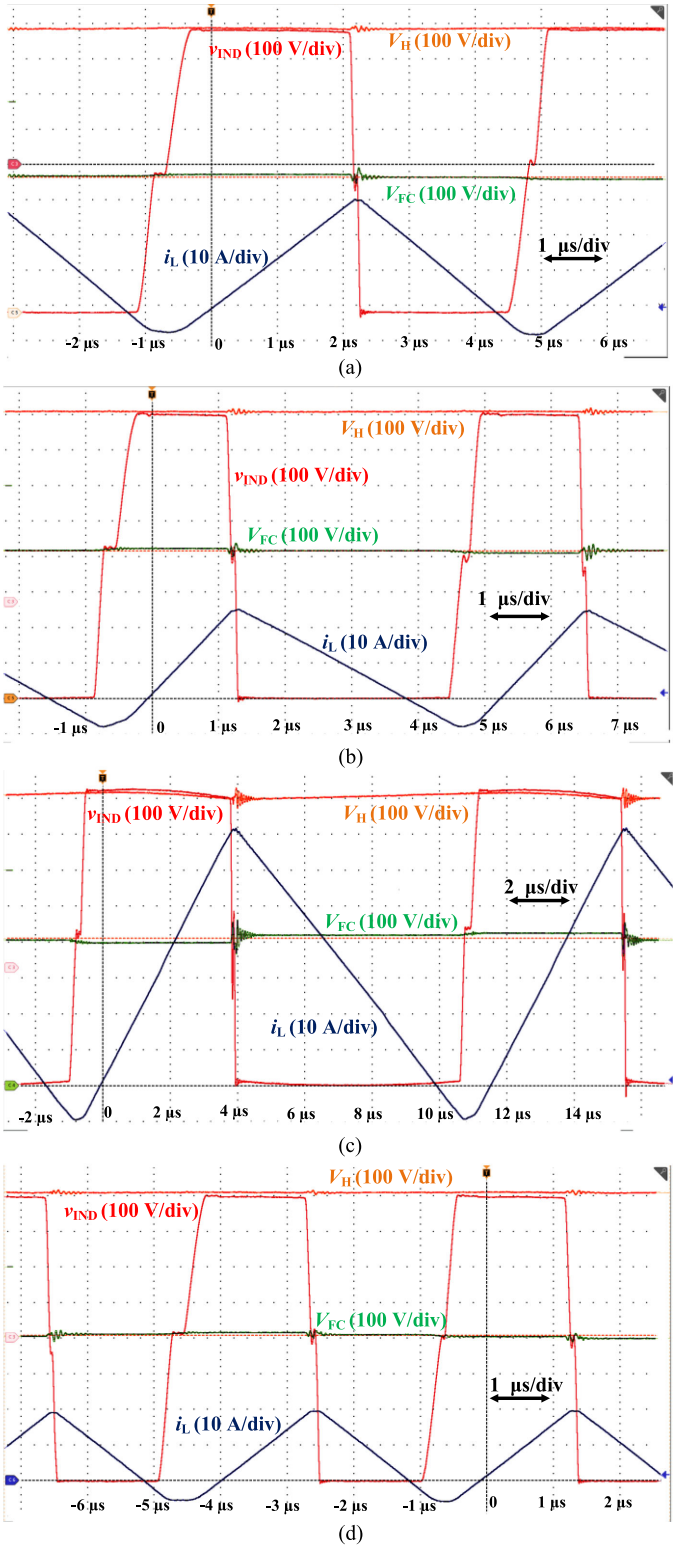

Fig. 14. Experimental results from an experiment performed at 800 V dc input voltage. From the top: input voltage (V_H); inductor voltage (v_{IND}) and current (i_L); flying capacitor voltage (V_{FC}). (a) Voltage gain G_V at 0.5 with resistance of 34.6 Ω–5.2 kW power at 178 kHz frequency. (b) Mode B (voltage gain G_V at 0.4) with a load resistance of 34.6 Ω - roughly 3.5 kW power at 189 kHz switching frequency. (c) Mode B (voltage gain G_V at 0.4) with a load resistance of 10.4 Ω - roughly 10 kW power at 86 kHz switching frequency. (d) Mode B (voltage gain G_V at 0.4) with a load resistance of 69.2 Ω - roughly 2.4 kW power at 254 kHz switching frequency.

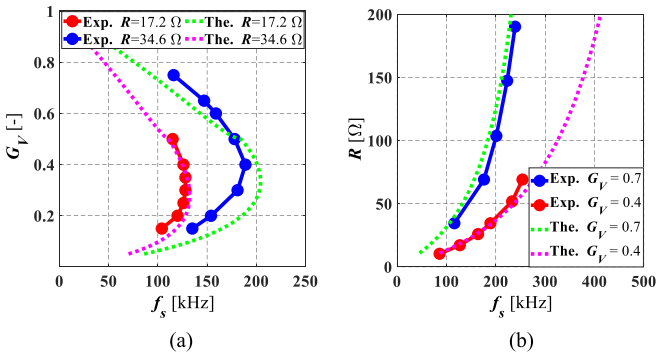

Fig. 15. Control characteristics – experimental (exp.) and theoretical (the.) comparison: (a) dependence between voltage gain G_V and switching frequency f_S; (b) dependence between load resistances R and switching frequency f_S.

switching frequency. At this G_V formulas for both modes are applicable and result in a situation where $t_{DT1} = t_{DT3}$ (see Figs. 3 and 5), thus resulting in near-sinusoidal shape of the inductor current near I_{MIN} value. The oscillogram shows balanced V_{FC} voltage, inductor current i_L and voltage v_{IND} and input voltage V_H. In this experiment, the inductor current established at 18 A rms and 39 A peak-to-peak values and the flying capacitor voltage ripples settled below 5%.

In the final test, performed at the same resistance (34.6 Ω), and at this voltage (800 V), presented in Fig. 14(b), the converter operated in mode B (voltage gain G_V at 0.4) at roughly 3.5 kW power and 189 kHz switching frequency. The presentation is identical as before. The inductor current established at 13 A rms and 33 A peak-to-peak values and the flying capacitor voltage ripples established below 5%.

The next oscillogram, shown in Fig. 14(c), presents a test in which the converter operated at lower resistance of 10.4 Ω. The experiment was performed at 800 V dc input voltage, in mode B (voltage gain G_V at 0.4) resulting in roughly 10 kW power at 860 kHz switching frequency. Again, the exposition is similar, with the image showcasing balanced V_{FC} voltage, inductor current i_L and voltage v_{IND}, as well as input voltage V_H. The inductor current established at 41 A rms and 82 A peak-to-peak values and the flying capacitor voltage ripples established below 5%.

The last oscillogram, presented in Fig. 14(d), depicts a test with the highest tested frequency (254 kHz). The experiment was performed at 800 V dc input voltage, in mode B (voltage gain G_V at 0.4) and with a resistance of 69.2 Ω resulting in roughly 2.4 kW. The inductor current established at 11 A rms and 25 A peak-to-peak values and the flying capacitor voltage ripples established below 5%.

Based on the experimental data acquired from the tests, a series of converter characteristics were plotted and are shown in Fig. 15. At first, in Fig. 15(a) the control characteristics showcasing the dependence between voltage gain G_V and switching frequency f_S for constant load resistances of 17.2 and 34.6 Ω are presented and the experimental results are compared to theoretical values calculated for the same operating parameters. As can

be seen, these are highly comparable, with slight differences in regard to voltage gain values. Nevertheless, the validity of the theoretical analysis of the converter and the control method is confirmed. In such conditions, the converter can operate at any voltage gain adopting proper frequency in range from dc to roughly 200 kHz for 34.6 Ω, and from dc to approximately 150 kHz for 17.2 Ω. In Fig. 15(b), the dependence between switching frequency f_S and resistances R for constant voltage gain of 0.4 (mode B) and 0.7 (mode A) is shown. Similarly to the situation before, the results from the experimental study are akin to the theoretical values. Furthermore, it should be noted that for such inductor (30 μH) higher resistance will result in very high operating frequencies leading to possible practical issues.

Next on, efficiency curves of the converter were plotted as well for the results from the experimental study and also according to theoretical derivations. Driving, control and forced 'cooling power losses settled at roughly 15 W and were omitted for efficiency characteristics for both theoretical and experimental cases, as these systems were supplied from a different source in the prototype tests. Furthermore, capacitor power losses were omitted as well.

The theoretical efficiency can be calculated as shown below, again with the omission of transition DT states. First, the inductor power losses was estimated as conduction wire loss $P_{\mathrm{C(L)}}$ using dc inductor resistance measured experimentally and (28) along with the inductor core loss $P_{\mathrm{core(L)}}$, which according to the software from the core manufacturer Ferroxcube can be estimated as constant 15 W, as variances for different operating points were minimal. As the inductor was constructed using Litz wires with high strand number, and to simplify the equations, other power losses, e.g., these caused by skin effect, were omitted

$$P_L = P_{C(L)} + P_{\mathrm{core}(L)} = R_{\mathrm{dc}(L)} {I_{\mathrm{rms}(L)}}^2 + P_{\mathrm{core}(L)}. \quad (33)$$

The other crucial source of the converter power losses are semiconductor power devices. Since low-pair transistors T_{L1} and T_{L2} are fully soft switched at turn-OFF, and achieve near-ZCS at turn-ON, their power loss is limited to conduction loss and using $R_{\mathrm{DS(on)}}$ from the datasheet at junction temperature of 100 °C and (27), it can be described as

$$P_{TL} = P_{C(TL)} = R_{\mathrm{DS(on)}} {I_{\mathrm{rms}(TL)}}^2. \quad (34)$$

When high-pair transistors are considered the conduction loss can be calculated using analogous relationship of $R_{\mathrm{DS(on)}}$ and (26). However, these power devices are hard-switched at turn-OFF and, thus, switching power loss at turn-OFF is added as well using the calculation based on datasheet values

$$P_{\mathrm{SW\_OFF}(TH)} = \frac{V_{\mathrm{DS}} I_{\mathrm{MAX}}}{V_d I_d} E_{\mathrm{OFF}} f_S \quad (35)$$

$$P_{TH} = R_{\mathrm{DS(on)}} {I_{\mathrm{rms}(TH)}}^2 + P_{\mathrm{SW\_OFF}(TH)}. \quad (36)$$

Finally, the converter theoretical efficiency can be calculated as

$$\eta = \frac{P_{\mathrm{conv}}}{P_{\mathrm{conv}} + (2P_{TH} + 2P_{TL} + P_L)} 100\%. \quad (37)$$

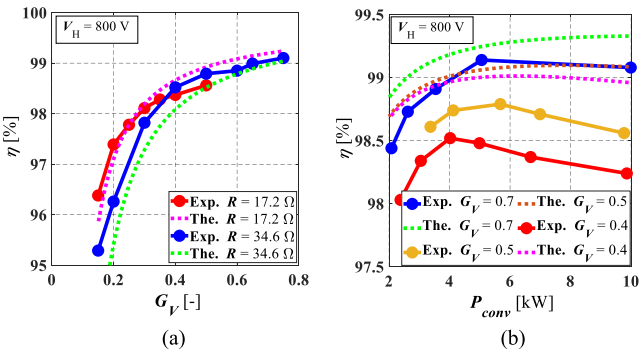

Fig. 16. Efficiency characteristics – experimental (exp.) and theoretical (the.) comparison: (a) dependence between converter efficiency η and voltage gain G_{V} (b); dependence between converter efficiency η and converter power P.

Fig. 16(a) presents the dependence between converter efficiency η and voltage gain G_{V} for constant load resistances of 17.2 and 34.6 Ω. As can be seen, the higher the gain, the higher the efficiency, reaching as high as 99.1%. The performed tests from G_{V} at 0.15 to 0.75 resulted in efficiencies in the range of 95.4 to 99.1%. The second characteristic, shown in Fig. 16(b), presents the dependence between converter efficiency η and converter power P_{conv} for constant voltage gains of 0.4, 0.5 and 0.7. For such operating conditions, for which the system was designed, the efficiency ranged from roughly 98% to 99% with peak efficiency of 99.1% at $G_{\mathrm{V}} = 0.7$ and $P = 5$ kW, which is a noteworthy value in comparison to other converters with similar voltage/current conditions, especially considering that the converter can operate for various voltage gains and a wide load range. When we compare the experimental results with the theoretical curves we can see that, similarly to the case before, these are in accordance as well.

VI. Comparison

A comparison of the FCC with the proposed TCM-Q2L control method with classic and state-of-the-art dc–dc converter topologies is presented in Table IV. When compared in terms of power semiconductor devices, even in unidirectional mode, four transistors are used. Furthermore, since the system is 3L, the voltage stress on the transistors is limited to $V_{\mathrm{H}}/2$. However, since the flying capacitor is used only for very brief moments of the switching cycle, the capacitance and the current flowing through the FC are greatly reduced in comparison to classic 3L FCC systems [33]. Moreover, even if the converter operates at very high frequency, due to the TCM-Q2L modulation pattern, the efficiency is at a very high level, which is comparable, or even surpasses the other approaches. Additionally, it is worth noting that this system does not require any additional components—the basic topology is identical as in a standard 3L FCC. Also, in order to facilitate the TCM-Q2L method and achieve soft switching it is required that the converter operates in near-CRM mode, thus, rms current values are quite high in comparison to the converters operating in CCM resulting in higher conduction loss.

TABLE IV
COMPARISON OF THE TCM-Q2L CONVERTER WITH OTHER TOPOLOGIES

Parameter	Basic 2L converter	CL-TCM converter [31]	3L FCC in CCM [33]	TCM-3L FCC [34, 36]	Proposed TCM-Q2L FCC
MOSFET no.	1	3	2	4	4
Diode no.	1	1	2	0	0
$V_{DS\ max}$	V_H	V_H	$V_H/2$	$V_H/2$	$V_H/2$
Switching frequency	Medium	Medium	Medium	Very high	Very high
Conduction mode	All	near-CRM	CCM	near-CRM	near-CRM
Soft switching	None	Full	None	Full at turn-on, partial at turn-off	Full at turn-on, partial at turn-off
Additional soft switching components	-	Yes	-	No	No
Flying capacitance	-	-	High	High	Very low
Choke inductance	Very high	Medium	Low	Low to medium	Medium to high
RMS choke current	Low	High	Low	High	High
Efficiency	Medium	High	Very high	Very high	Very high

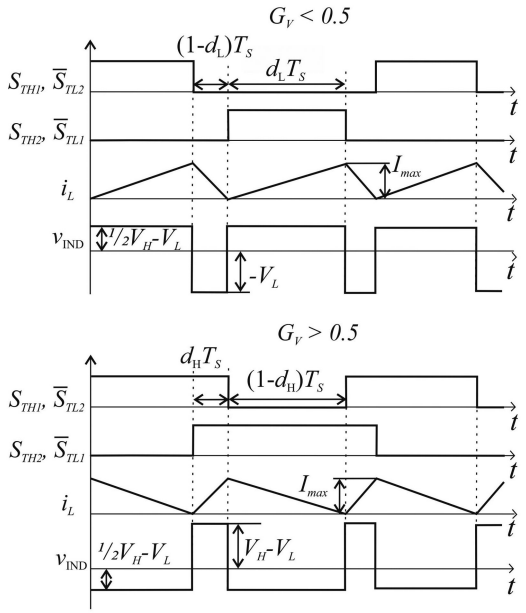

Fig. 17. Waveforms for conventional 3L buck converter with flying capacitor for $G_V < 0.5$ and $G_V > 0.5$.

Furthermore, the third level of voltage is employed only to balance the FC voltage and achieve soft switching and not to lower the inductor current derivative as it is the case for a conventional 3L converter. Moreover, the methodology for achieving soft switching is similar as in a TCM-3L converter [34], [38], but in that solution the inductor value will be lower than in TCM-Q2L. However due to Q2L operation both current and the capacitance of the FC is reduced.

In order to compare these two systems more comprehensively further theoretical analysis was conducted. The assumption is that, in order to simplify the equation derivation, the TCM intervals, in which the resonance occurs, are omitted for both converters, as the length of these intervals is highly comparable for both Q2L and 3L converters and their impact on system operating frequency and RMS currents is limited for high output power. The voltage and current waveforms for a conventional 3L converter operating in CRM are shown in Fig. 17. It can be noted that depending on the voltage gain G_V the modulation is different. For $G_V < 0.5$

$$\Delta i_L = \frac{(1/2V_H - V_L)\, d_L T_S}{L} \tag{38}$$

$$d_L\,(1/2V_H - V_L) = (1 - d_L)\, V_L. \tag{39}$$

For $G_V > 0.5$

$$\Delta i_L = \frac{(V_H - V_L)\, d_H T_S}{L} \tag{40}$$

$$d_H\,(V_H - V_L) = (1 - d_H)\,(V_L - 1/2V_H)\,. \tag{41}$$

While for the Q2L operated converter, under the previously mentioned assumptions, the ripples are regardless of the voltage gain and the switching frequency and can be described as

$$\Delta i_L = I_{\mathrm{MAX}} = 2I_O. \tag{42}$$

In CRM, the ratio between the output current I_O and max inductor current I_{MAX} is constant for all operating points and equal to 1:2 and the output power of the system is controlled by its operating frequency. Assuming that $\Delta i_L/I_O = 2$, the inductor ripple frequency (which is doubled in comparison with the switching frequency in the conventionally operated 3L converter) can be described as

$$f_{\Delta i_L} = \frac{R(1 - 2G_V)}{2L} \text{ for } G_V \le 0.5 \tag{43}$$

$$f_{\Delta i_L} = \frac{R(1 - G_V)(2G_V - 1)}{2LG_V} \text{ for } G_V \ge 0.5. \tag{44}$$

For the proposed TCM-Q2L converter, omitting the resonance intervals, the inductor ripple frequency can be described by the same equation as for a conventional 2L buck converter operating in CRM

$$f_{\Delta i_L} = \frac{R(1 - G_V)}{2L}. \tag{45}$$

According to the characteristics shown in Fig. 18 3L-based converter operates at much lower inductance with the same inductor current ripples. However, it does not necessarily eliminate the Q2L method. First, the regulatory characteristic (effectively frequency) of the 3L system is highly nonlinear for $G_V \ge 0.5$,

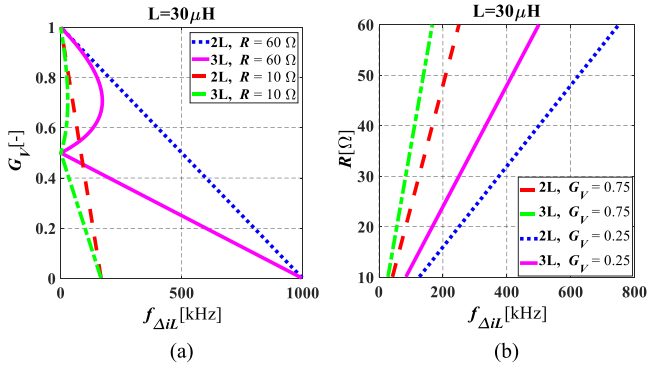

Fig. 18. Ideal characteristics for inductor ripple frequency for 2L and 3L FCCs with the same inductance and with the omission of soft-switching operation –(a) voltage gain dependence on frequency; (b) load resistance dependence on frequency.

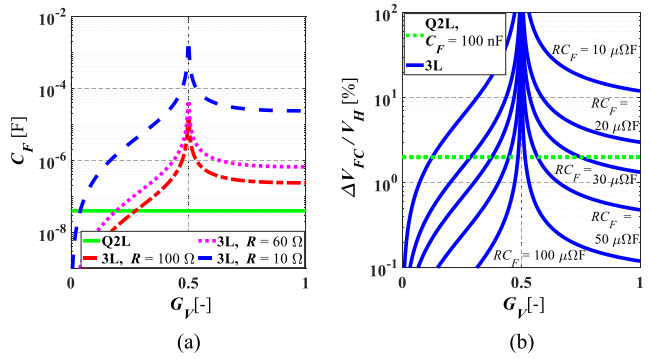

Fig. 19. Ideal characteristics for flying capacitance for Q2L and 3L FCCs with the omission of soft-switching operation. (a) Flying capacitance dependence on voltage gain for identical flying capacitor voltage ripples at 5% of V_{H}. (b) Flying capacitor voltage ripples dependence on voltage gain for various RC_{F} values (b).

which may impose problems in terms of system control. Second, based on the assumptions that V_{FC} is constant and equal to $V_{\mathrm{H}}/2$, the 3L converter cannot effectively operate near $G_{\mathrm{V}} = 0.5$ as that would lead to very low frequencies (theoretically $f_{\mathrm{S}} = 0$ for $G_{\mathrm{V}} = 0.5$) and, finally, both system operate at a very wide frequency range for different voltage gains, which is an issue for the 3L system in terms of the flying capacitor, as for varied voltage gain, thus varied switching frequency, the flying capacitor voltage ripples will be very high and can be described as

$$\frac{\Delta V_{\mathrm{FC}}}{V_H} = \frac{I_{\max} d_L T_S}{2 C_F I_O R} = \frac{2 G_V}{C_F f_S R} \text{ for } G_V \leq 0.5 \tag{46}$$

$$\frac{\Delta V_{\mathrm{FC}}}{V_H} = \frac{I_{\max} d_H T_S}{2 C_F I_O R} = \frac{2(1 - G_V)}{C_F f_S R} \text{ for } G_V \geq 0.5. \tag{47}$$

Comparison between the flying capacitor value for Q2L and 3L systems can be carried out correlating (46) and (47) with (30).This is presented in Fig. 19, where the converters operate with frequencies according to Fig. 18(a) and with the assumption that both converters have the same flying capacitor voltage ripples ΔV_{FC} at 5% of voltage V_{H} [see Fig. 19(a)]. Moreover, Fig. 19(b) showcases further comparison between voltage ripples and voltage gain and various values of RC_{F}. As shown, the flying capacitance in the Q2L system is very low and constant regardless of load resistance R. On the other hand, in the 3L system it is dependent on the operating point and much higher for most of the range. This is especially visible for low load resistances, where the difference is very significant. Moreover, near $G_{\mathrm{V}} = 0.5$ the 3L system requires very high flying capacitance C_{F} for lighter loads, thus imposing whether 3L systems can be practically used for such voltage gains, whereas for the Q2L system this is a nonexistent issue. Furthermore, using a flying capacitor with lower capacitance provides the possibility to reduce the stray inductance of the switching loop connections, which will improve the switching processes of the hard-turned-OFF transistors T_{H1} and T_{H2}.

According to this comparison TCM-Q2L will be superior for high-power application with light loads and for voltage gains close to $G_{\mathrm{V}} = 0.5$, as compared with TCM-3L the increase in terms of inductance L is not as high as the possible gain based on lowering the flying capacitance.

Moreover, since both solutions operate on a very similar basis in terms of TCM and variable operating frequency the efficiency should be similar as well. In regard to the rms currents, since the current waveforms are alike in both systems, (26) and (27) are true for TCM-3L as well, thus the semiconductor power loss is highly comparable. The differences can be observed in FC power loss, as in the TCM-Q2L system the FC current is minimal, however the impact of FC loss is not a significant factor compared to semiconductor and inductor losses.

The case is alike in comparison to the system shown in [37], since the TCM operation is very similar here and the characteristics in shown in Fig. 18 are applicable as well. The difference comes in a fact that the system in [37] has a different topology, as it essentially is a doubled 2L buck converter, and thus, there is no flying capacitor. Moreover, there are two high voltage side capacitors instead of one, however rated at a lower voltage of $V_{\mathrm{DC}}/2$. Finally, the converter in [37] operates without capacitor voltage measurement.

Altogether, when compared with other conventional and state-of-the-art solutions the TCM-Q2L converter can match or even surpass its competitors in terms of performance and is a noteworthy solution in high-power dc–dc energy conversion.

VII. Conclusion

In this article, a novel TCM-Q2L control method for a flying capacitor converter have been proposed. Based on an extensive theoretical analysis, simulation study, and experimental tests on the constructed prototype up to 1500 V voltage and up to 10 kW power the proposed system has been successfully validated. The efficiency of the converter peaked at 99.1% for 5 kW output power, voltage gain of 0.7 and very high operating frequency at 189 kHz, while maintaining the efficiency above 97.8% for most of the operating range. Furthermore, Q2L operation mode have provided the possibility to use fast, affordable and widely available 1200 V SiC MOSFETs at 1500 V input voltage with intensively reduced flying capacitance, to just 330 nF, which is

a minimal value in comparison with more standard approaches. Moreover, the proposed TCM-Q2L modulation pattern introducing full-ZVS conditions for turn-ON provides the possibility to operate at very high frequencies, even as high as 250 kHz, thus maintaining a low value of inductance, while keeping the efficiency very high. Finally, the system is capable of operation for a wide variety of voltage gains and loads.

Thus, applying the proposed TCM-Q2L control for the FCC may be a noteworthy solution to convert energy in MV range with high efficiency and relatively high power density, and may be competitively used against classical two-level, as well as three-level and series connection-based dc–dc converters.

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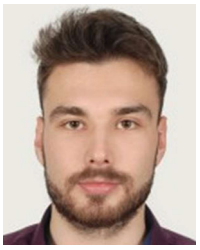

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3.5 Investigation of Soft-Switching QSW Technique in DC/DC SiC-Based Flying Capacitor Converter With Q2L Control [P5]

[P5] **R. Kopacz**, M. Harasimczuk, P. Trochimiuk and J. Rąbkowski, "Investigation of Soft-Switching QSW Technique in DC/DC SiC-Based Flying Capacitor Converter With Q2L Control," in IEEE Transactions on Industrial Electronics, vol. 70, no. 9, pp. 9035-9045, Sept. 2023. Points according to the Ministry of Education and Science: **200**, Impact Factor: **8.162**. Contribution of the dissertation author: **50%**. [133]

Investigation of Soft-Switching QSW Technique in DC/DC SiC-Based Flying Capacitor Converter With Q2L Control

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***Abstract*—This article investigates the soft-switching quasi-square-wave (QSW) technique in dc/dc SiC-based flying capacitor converter with quasi-two-level (Q2L) control establishing design guidelines for constructing high-efficiency soft-switched bidirectional converters with low-voltage power transistors. The general idea behind the soft-switching in the proposed system is based on near critical conduction mode operation using TCM (triangular current mode) and Q2L control with the addition of auxiliary transistor capacitances. The soft-switching process is based on a resonance between the capacitances in parallel to each transistor, and the main inductor—ZVS at turn ON is ensured through proper modulation pattern according to TCM-Q2L control, and the turn-OFF soft-switching mechanism is assured through the novelty in the form of adding auxiliary capacitance in parallel to each of the SiC power MOSFETs according to the QSW operation. Thus, the converter can reach very high efficiency (peak at 99.5%), maintaining soft-switching for a wide operating range, using only small auxiliary SMD capacitors and a low-volume flying capacitor, leading to high power density. The presented study is based on experimental tests using a 1.5 kV model at up to 15 kW and includes the impact of various auxiliary capacitance values and optimal capacitor value selection for maximizing the converter efficiency.**

***Index Terms*—DC–DC power conversion, power converter, power electronics, power MOSFETs, zero-voltage switching.**

I. Introduction

THE constant demand to preserve energy and limit greenhouse gas emissions is often addressed through renewable energy sources. To fully exploit solar and wind sources regardless of the time of the day and other factors induced by natural causes, employing energy storage systems is necessary. Therefore, there is a great need to implement highly efficient and flexible energy conversion systems, usually mainly comprising power converters. Specifically, dc/dc nonisolated converters can be named crucial since dc technology is intensively developed throughout all electric systems, in medium voltage range, and especially for the mentioned energy storages, as well as for photovoltaics, electric transport, and others.

Since establishing high efficiency is one of the most sought parameters of power converters, preferably with high power density, soft-switching-based systems are often the most common choice for applications with such requirements, as they provide low power loss and EMI levels that lead to more compact and more efficient designs. Moreover, wide-bandgap power devices, e.g., SiC, currently commonly employed in state-of-the-art systems, due to their fast-switching capabilities associated with high voltage ratings, are susceptible to substantial *dv/dt* ratios. This, in combination with inevitable stray inductances and capacitances in the power switching loop of the converter, leads to various issues, including overshoots and oscillations resulting in high EMI generation, often unaccepted in power converter applications [1], [2], [3]. Therefore, slowing down the SiC power transistors is usually necessary to adapt to the required norms and standards, leading to incomplete utilization of the SiC transistors and their many benefits. Indeed, employing additional *dv/dt*-limiting measures is a viable solution, but it comes with a price of more complexity and/or lower power density. In this case, using soft-switching topologies also helps to fully utilize the many advantages of the SiC power devices without any supplementary additions compared to conventional hard-switched converters. Many approaches to reach soft-switching in nonisolated systems can be identified [4], [5], [6], [7].

Conventional soft-switched converters with resonant [6], [8], [9], [10], [11] and quasi-resonant [12] cells provide satisfactory performance with high efficiencies. However, they generally require additional, often bulky, components in the resonance circuit and introduce the addition of circulating currents. Thus, they may induce low power densities and extra conduction power losses. Moreover, they are usually bound to a specific operating point and its near vicinity to achieve the highest efficiency, eliminating them from use in some applications that require various voltage gain levels or work with a wide array of loads.

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Zero-voltage transition (ZVT) converters [6], [13], [14], [15], [16] provide the possibility to obtain more universal conditions for soft-switching using auxiliary resonance circuits for each switch. Thus, operation in wide load and voltage gain is available. Alas, adding supplementary resonance components in the form of active snubber cells comprised of additional switches and/or other passive components of considerable volume is necessary, leading to lowered power density of the system, often also with enlarged voltage stress on snubber components and/or the requirement of more sophisticated gate drivers [13]. Therefore, this solution is also nonideal, as the total component count is high, and the volume is on a significant level.

Quasi-square-wave (QSW) operation [17], [18], [19], [20], also often included in triangular current mode (TCM) controlled converters [21], [22], [23], [24], incorporates the converter filter inductor and the output transistor capacitances as the resonant network, thus limiting the requirement of additional components in the converter to reach zero-voltage switching. Here, conventional approaches to TCM-based control can be named in both three level (3L) [18], [23] and Q2L [21] variants. In such systems, higher power density can be achieved compared to other, more conventional approaches to soft-switching converters, where supplementary components are apparent. Alas, since the resonant inductor is also the main component in the energy path, and the converters are required to be operated in near-critical conduction mode (CRM) or discontinuous conduction mode (DCM), the current ripples are on a significant level, leading to increased conduction losses and higher output voltage ripples compared to conventional systems operating in continuous conduction mode (CCM). However, output voltage ripples can be minimized through a multiphase configuration, which is a well-known practice for CRM and DCM-operated systems. Moreover, to effectively work in a wide operating range, such converters must be controlled with a variable frequency, leading to some complications in the control system. Furthermore, the output capacitance of the MOSFET is not sufficient to provide full ZVS also at turn OFF, which results in some remnant switching power losses. Thus, even considering the fact that the turn-OFF switching losses are smaller than the already-eliminated turn-ON loss due to high operating frequencies, the switching loss is still visible.

Therefore, in the proposed system, the addition of small supplementary capacitors, with values in the span of single nanofarads, in parallel to each of the transistors, as a turn-OFF snubber circuit, similarly as in [25] and [26], is suggested to provide full soft-switching, also at turn OFF, for the TCM-operated converter. Such a novelty is a viable option to ensure full ZVS conditions for the power devices with a minor increase in component count and minimal impact on converter volume. Furthermore, the inclusion of these capacitors, additionally to providing soft-switching, also helps to limit the *dv/dt* ratios of the transistors as the voltage rise time is intensively extended, and the slopes at which the v_{DS} voltage change are much less steep, resulting in less EMI issues. Thus, applying the QSW technique is a simple solution to both *dv/dt*-based limitations of SiC power transistor usage and achieving low power losses with a single measure. While the QSW technique applied for full soft-switching through auxiliary capacitors is not a new idea [20], its use in modern SiC-based dc/dc converters, especially Q2L-controlled, where the issues related to *dv/dt* ratios of the transistor are crucial, has not been shown in the literature yet, while it shows many benefits compared to other state-of-the-art converters, including three-level flying capacitor converters with a conventional approach to TCM operation with only partial soft-switching, both in Q2L and 3L systems.

Thus, in this article, an investigation into applying QSW-based soft-switching to a Q2L-controlled flying capacitor converter (FCC) and its possible benefits is presented, which results in an ultra-low-power loss dc/dc converter, based on the flying capacitor structure, TCM-Q2L control, and the novelty for the SiC-based system, in the form of auxiliary capacitance providing ZVS, also at turn OFF, providing efficiency reaching as high as 99.5% along with minimal component count and satisfactory power density dealing with the issue of nonfull soft-switched operation of the conventional TCM-operated converters. The core focus of the article, and its main contribution, is the addition of small capacitors in parallel to each MOSFET, ensuring full ZVS for the TCM-Q2L FCC throughout a wide operating range. Moreover, establishing design guidelines and optimal capacitor values for maximizing system efficiency and restricting the transistor *dv/dt* leading to lower EMI generation and ensuring full utilization of the SiC power devices is also concerned. The proposed converter can be effectively employed in various unidirectional and bidirectional dc-based systems, especially in photovoltaics, dc microgrids, and energy storage systems, while the prototype showcased in this article is dedicated to 1500-V dc applications.

The structure of the publication is as follows. After the introduction showcasing a brief overview of soft-switching converters and portrayal of the investigated system, a description of the operation principles of the converter is presented in Section II. The following Section III contains design guidelines, including the study of C_{aux} impact and its optimal value selection, the experimental study showcasing the prototype, its control and efficiency characteristics for various C_{aux} values, and complete results for the optimal capacitance at peak power of 15 kW. Then, Section IV compares the performance of the presented converter with other state-of-the-art approaches. Finally, the article is concluded in Section V.

II. QSW-Soft-Switched Flying Capacitor Converter With Q2L Control

A. Operation Principles

The proposed converter is strictly based on the TCM-Q2L flying capacitor converter introduced in [21] and [22], which incorporates ZVS at turn ON using the TCM technique [18], and the Q2L method to reach higher converter voltages using low-voltage power devices in stack, as it shows good performance compared to conventional multilevel or series-connection approaches [27]. The converter scheme is shown in Fig. 1 with the main contribution of this article, the inclusion of auxiliary capacitors is parallel to each of the transistors employed to assure

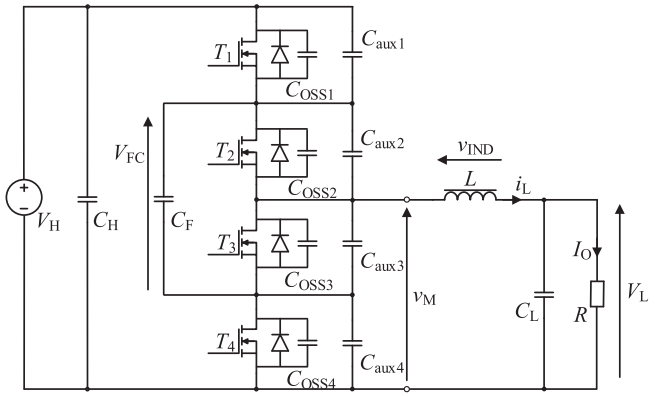

Fig. 1. Scheme of the TCM-Q2L FCC with auxiliary capacitors in parallel to each MOSFET.

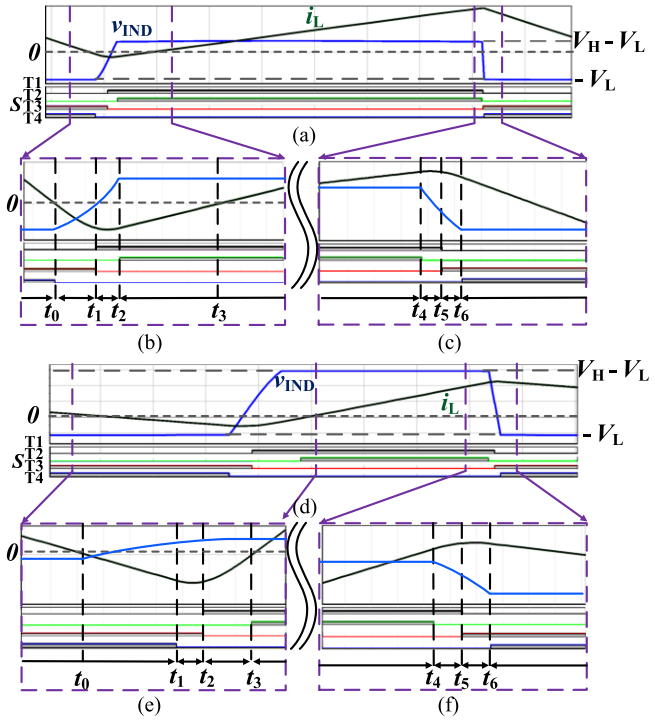

Fig. 2. (a) Modulation pattern for TCM-Q2L converter: mode A—general view. (b) Low current transition. (c) High current transition. (d) Mode B—general view. (e) Low current transition. (f) High current transition.

full ZVS operation according to the QSW technique, which will be elaborated on further in this article.

The operation principles of the converter can be divided into seven intervals, as shown in Fig. 2 and further described according to the switching states in Table I. Here, only one exemplary transition is shown for the analysis. However, to have the converter operate properly, an alternating modulation pattern [21] employing the same operating principles has to be used. To simplify the analysis of the converter operation, constant voltages on capacitors C_H, C_F, and C_L during one switching period are assumed. Moreover, transistor turn ON, turn-OFF times, and parasitic parameters of all elements except

TABLE I
TRANSISTOR SWITCHING STATES IN REFERENCE TO FIG. 2

Interval (mode A)	Interval (mode B)	T_1	T_2	T_3	T_4	v_M	Status
Basic two-level (2L) switching states							
$t_2 - t_4$	$t_3 - t_4$	1	1	0	0	V_H	Energy transfer from V_H
$t_6 - t_0$	$t_6 - t_1$	0	0	1	1	0	Output charged from L
Supplementary switching states							
$t_1 - t_2, t_4 - t_5$	$t_2 - t_3, t_4 - t_5$	1	0	0	0	*var*	Transition 1
-	-	0	1	0	0	*var*	Transition 2
$t_0 - t_1, t_5 - t_6$	$t_1 - t_2, t_5 - t_6$	0	0	1	0	*var*	Transition 3
-	-	0	0	0	1	*var*	Transition 4

the output capacitances C_{OSS} of the transistors are omitted. These capacitances were assumed to be constant in the whole voltage range and, along with auxiliary capacitances C_{aux}, equal for all the transistors. The operation of the converter depends on voltage gain ($G_V = V_H/V_L$); therefore, the operation was divided into mode A for voltage gain $G_V \geq 0.5$ and mode B for $G_V \leq 0.5$. Furthermore, the addition of auxiliary capacitances C_{aux} enlarges the capacitance that needs to be recharged at the turn-ON process of each transistor. Thus, to effectively employ the equations described above, the sum capacitance comprised of the output transistor capacitance and the additional C_{aux} capacitance needs to be used.

Interval 1 ($t_0 - t_1$) Fig. 2(a), (b) (mode A); 2(d), (e) (mode B): Before the considered interval transistors T_1 and T_2 are OFF, transistors T_3 and T_4 are ON. Current in inductor L is reducing linearly. Further operation of the converter depends on voltage gain. In mode A, transistor T_4 is turned OFF at time t_0 and zero voltage, and it causes resonant operation between capacitances C_{oss1}, C_{oss4}, C_{aux1}, C_{aux4}, and inductance L. Inductor current in the considered interval and mode A can be described by

$$i_{L(A)}(t) = \frac{-V_L}{Z}\sin(\omega_r t) \tag{1}$$

where $Z = (L/C_{eq})^{1/2}$, $\omega = 1/(LC_{eq})^{1/2}$, $C_{eq} = 2C_{oss} + 2C_{aux}$.

Resonant operation in the considered interval allows reducing voltage on transistor T_1, enabling its turn ON at zero voltage at time $t_{1(A)}$. Interval ends when the voltage on transistor T_1 reaches zero and can be described by the following equation:

$$t_{1(A)} - t_0 = \cos^{-1}\left(\frac{G_V - 1/2}{G_V}\right)\frac{1}{\omega_r}. \tag{2}$$

Unlike in mode A, in mode B, transistor T_1 remains ON during the considered interval, which allows for linear reduce the current of inductor L. Transistor T_1 turns OFF at time $t_{1(B)}$ at the value of inductor current, which allows us to completely discharge capacitances C_{oss1}, C_{oss2}, C_{aux1}, C_{aux2} at successive intervals and turning ON transistors T_1 and T_2 at zero voltage. The considered interval in mode *B* can be described by the following equations:

$$t_{1(B)} - t_0 = -\frac{i_L(t_{1(B)}) \cdot L}{V_L} \tag{3}$$

$$i_L(t_{1(B)}) = -\frac{V_H\sqrt{1 - 2G_V}}{Z}. \tag{4}$$

Interval 2; ($t_1 - t_2$), Fig. 2(a), (b) (mode A); 2(d), (e) (mode B): In mode A, transistor T_1 is ON, and other transistors are OFF. During this interval, capacitances C_{oss2} and C_{aux2} are discharging, and C_{oss3} and C_{aux3} are charging. At the end of the interval, transistor T_2 turns ON at zero voltage. The considered interval can be described by the following equations:

$$i_{L(A)}(t) = \frac{-V_L}{Z} \sin\left\{\omega_r\left[t + (t_{1(A)} - t_0)\right]\right\} \tag{5}$$

$$t_{2(A)} - t_{1(A)} = \cos^{-1}\left(\frac{G_V - 1}{G_V}\right)\frac{1}{\omega_r} - \left(t_{1(A)} - t_0\right). \tag{6}$$

In mode B, the interval starts by turning OFF transistor T_4. Capacitances C_{oss4}, C_{aux4} are charging, and capacitances C_{oss1}, C_{aux1} are discharging. At the end of the interval, transistor T_1 turns ON at zero voltage. The considered interval in mode B can be described by the following equations:

$$i_{L(B)}(t) = \frac{-V_L}{Z} \sin\left\{\omega_r(t) + \sin^{-1}\left[-i_L(t_{1(B)})\right]\right\} \tag{7}$$

$$t_{2(B)} - t_{1(B)} = \cos^{-1}\left(\frac{G_V}{G_V - 1}\right)\frac{1}{\omega_r} - \left(t_{3(B)} - t_{2(B)}\right). \tag{8}$$

Interval 3 (t_2–t_3) Fig. 2(a), (b) (mode A); 2(d), (e) (mode B): In mode A, the considered interval starts by turning ON at zero voltage transistor T_2, and the inductor current starts to flow linearly according to the equation:

$$i_{L(A)}(t) = i_L(t_{2(A)}) + (V_H - V_L) \cdot t/L. \tag{9}$$

At the end of the interval, the inductor current is equal to zero, and the interval can be given by

$$t_{3(A)} - t_{2(A)} = -\frac{i_L(t_{2(A)}) \cdot L}{V_H - V_L} \tag{10}$$

$$i_L(t_{2(A)}) = -\frac{V_H\sqrt{1 - 2G_V}}{Z}. \tag{11}$$

In mode B, interval starts by turning ON transistor T_1 at zero voltage. Operating conditions of the converter are similar to interval 2, mode A. Interval and inductor current in the considered interval can be calculated by the following equation:

$$i_{L(B)}(t) = \frac{-V_L}{Z} \sin\left\{\omega_r(t) + \sin^{-1}\left[i_L(t_{2(B)})\right]\right\} \tag{12}$$

$$t_{3(B)} - t_{2(B)} = \cos^{-1}\left(\frac{1/2 - G_V}{1 - G_V}\right)\frac{1}{\omega_r}. \tag{13}$$

Interval 4; ($t_3 - t_4$), Fig. 2(a), (b), (c) (mode A); 2(d), (e), (f) (mode B): During the considered interval, transistors T_1 and T_2 remain ON. The inductor current rises linearly, and energy from the input voltage source is transferred to the inductor and load. Inductor current in the considered interval is given by

$$i_L(t) = \frac{V_H - V_L}{L}t. \tag{14}$$

Interval 5; (t_4 - t_5); Fig. 2(a), (c) (mode A); 2(d)., (f) (mode B): At time t_4, transistor T_2 is OFF, capacitances C_{oss2} and C_{aux2} are charging, and capacitances C_{oss3} and C_{aux3} are discharging. Thanks to the capacitor C_{aux2}, transistor T_2 is turning ON at zero voltage. Assuming constant inductor current in the considered interval, its length can be given by

$$t_5 - t_4 = \frac{V_H C_{oss}}{i_L(t_4)}. \tag{15}$$

Interval 6; ($t_5 - t_6$); Fig. 2(a), (c) (mode A); 2(d), (f) (mode B): At time t_5, transistor T_3 turns ON at zero voltage, transistor T_1 is OFF at zero voltage. During this interval, capacitances C_{oss1}, C_{aux1} are charging, and capacitances C_{oss4}, C_{aux4} are discharging. Assuming constant current in the whole interval, its span can be calculated by

$$t_6 - t_5 = \frac{V_H C_{oss}}{i_L(t_5)}. \tag{16}$$

Thanks to using additional output capacitors C_{aux1} and C_{aux2} in parallel with transistors T_1 and T_2, turn OFF at zero voltage is obtained, which is the main advantage compared to the conventional TCM-operated converters without additional capacitors. Furthermore, as capacitors C_{aux3} and C_{aux4} are connected parallel with transistors T_3 and T_4, zero-voltage switching operation is also assured in boost operation, not covered in this article.

Interval 7; (t_6 - t_0); Fig. 2(a), (b), (c) (mode A); 2(d), (e), (f) (mode B): At time t_6, transistor T_4 is turned ON at zero voltage. Inductor current reduces linearly; energy accumulated in the inductor is transferred to the load and can be given by

$$i_L(t) = i_L(t_6) - \frac{V_L}{L}t. \tag{17}$$

Therefore, the whole switching sequence for one soft-switching transition has been presented, showcasing full ZVS for all transistors, both at turn ON, due to the TCM operation, and turn OFF, thanks to additional C_{aux} capacitors.

B. Voltage Gain and Switching Frequency

In the converter with the proposed zero-voltage transistor turn-OFF technique, voltage gain G_{v} and switching frequency f_S were calculated based on the principle operation described by (1)–(16) and is not shown here due to its highly intricate structure. The model was more thorough than in [18] to calculate the voltage gain more precisely, as it also included the impact of the transition $t_4 - t_5$ and $t_5 - t_6$ states with the resonant operation.

Furthermore, switching frequency and voltage gain are described by different equations for mode A ($G_{\text{v}} \geq 0.5$) and mode B ($G_{\text{v}} \leq 0.5$). By entering additional parameters, duty cycle defined as simultaneous turn-ON transistors T_1 and T_2 time to switching period ratio and assuming constant current in inductor L in interval $t_4 - t_6$ equal $i(t_5)$ input and output power comparison for mode A can be described by

$$\frac{D_{(A)}V_H\left(i_L(t_5) + i_L(t_{2(A)})\right)}{2} = V_L I_O. \tag{18}$$

For mode B, it can be described by

$$\frac{D_{(B)}V_H i_L(t_5)}{2} = V_L I_O. \tag{19}$$

The maximum current in mode A can be described under the following equations:

$$\frac{D_{(A)}T_S\left(V_H - V_L\right)}{L} = i_L(t_5) - i_L(t_{2(A)}) \tag{20}$$

$$i_L(t_5) = \frac{V_L\left(\left(1 - D_{(A)}\right)T_S - \left(t_{2(A)} - t_0\right) - \left(t_6 - t_4\right)\right)}{L}. \tag{21}$$

For mode B, it can be described by

$$\frac{D_{(B)}T_S\left(V_H - V_L\right)}{L} = i_L(t_5) \tag{22}$$

$$i_L(t_5) = \frac{V_L\left(\left(1 - D_{(B)}\right)T_S - \left(t_{3(A)} - t_0\right) - \left(t_6 - t_4\right)\right)}{L}. \tag{23}$$

Based on (1)–(23), using MATLAB, the voltage gain and the switching frequency were determined numerically for different output resistance and auxiliary capacitances C_{aux} and are shown in Fig. 5 in Section III-C.

C. Soft-Switching Conditions

Furthermore, in order to assure ZVS at turn ON, the transistors have to switch when their respective output capacitances have already been discharged. This can be achieved through proper variable frequency control that sets specific times for the transistor states (dead times) at particular minimum inductor currents required to recharge the output capacitances. The equations for the mentioned times were shown before, while, in regard to the current, it depends on the voltage gain. In mode A ($G_{\text{V}} \geq 0.5$), transistors have to be turned OFF at the time when the inductor current reaches 0. On the other hand, in mode B ($G_{\text{V}} \leq 0.5$), this should occur at a specific current described by (4). Such an approach assures soft-switching at turn ON. However, contrary to conventional TCM-based systems, full ZVS at turn OFF is also attained in the proposed system using small auxiliary capacitors in parallel to each MOSFET, as shown in Fig. 1. In regard to the proper selection of C_{aux}, it will be elaborated on in the following section.

D. Voltage Balance Mechanism

In order to have the converter operating properly, the constant voltage on the flying capacitor equal to $V_{\text{H}}/2$ is required. Otherwise, the voltage across the transistors is not balanced, which may lead to the system's failure. This can be attained by employing the voltage balancing loop as in [21].

E. Voltage and Current Stress of Power Devices

Assuming constant voltage on flying capacitor C_{F} equal $V_{\text{H}}/2$ and omitting the negative effect of parasitic inductances on maximum voltage during switching semiconductors components, maximum voltage on transistors can be described by the following equation:

$$V_{DS\_\max(\text{T1,T2,T3,T4})} = V_H/2. \tag{24}$$

TABLE II
INTEGRAL BOUNDS FOR TRANSISTOR RMS CURRENT CALCULATION USING (25)

$T_{\text{X,m}}$	T_1,A	T_1,B	T_2,A	T_2,B	T_3,A	T_3,B	T_4,A	T_4,B
ta	$t_{1(A)}$	$t_{2(B)}$	t_6	t_0	$t_{2(A)}$	$t_{3(B)}$	t_5	t_5
tb	t_5	t_5	t_0	$t_{1(B)}$	t_4	t_4	$t_{1(A)}$	$t_{2(B)}$

RMS currents in converter components depending on voltage gain can be described according to the following equation:

$$I_{RMS(Tx,m)} = \sqrt{\frac{1}{T_S}\int_{ta}^{tb} i_L(t)^2 \mathrm{d}t} \tag{25}$$

where T_x is the transistor number with $x = 1, 2, \ldots, 4$; m is either A for mode A or B for mode B; and *ta* and *tb* are the integral bounds according to the previous equations and Table II.

Inductor RMS current is given by

$$I_{RMS(L)} = \sqrt{\frac{1}{T_S}\int_{0}^{Ts} i_L(t)^2 \mathrm{d}t}. \tag{26}$$

III. LABORATORY MODEL AND EXPERIMENTAL RESULTS

A. Converter Component Selection and Design Considerations

Proper selection of converter components is not trivial, especially in terms of auxiliary capacitances. While higher capacitances assure full zero-voltage switching (ZVS) at turn OFF, alas, they also lead to enlarged other power losses. As the output MOSFET capacitance is enlarged, the energy that needs to be recharged in that capacitance within the switching time of the transistors is higher as well. Therefore, the negative inductor current needs to reach lower values, the RMS value is higher, the resonant frequency is lower, and, consequently, the conduction loss is also enlarged. On the other hand, switching loss is significantly reduced. Furthermore, assuming the same inductance, longer times are required to recharge the higher capacitance and assure ZVS at turn ON, leading to reduced switching frequency. This may be deemed negative as, for voltage gains near 1 and 0, the current ripples are on a significant level. Therefore, in that regard, lower auxiliary capacitance values are preferable. In summary, the expected efficiency for the converter with C_{aux} could be lower for powers significantly lower than the rated power of the converter prototype.

Therefore, when designing a converter using the presented technique, it is recommended to perform an efficiency estimation using several auxiliary capacitor values, starting from the transistor output capacitance C_{OSS}, using the theoretical analysis shown in the next section. Employing such an approach provides an optimal capacitance value with minimum power loss for a specific application. Furthermore, the issue of capacitor tolerances is also noteworthy, as changes in capacitances directly affect the ZVS conditions, the operating frequencies, as well as the efficiency estimation used for capacitor value selection. However, this does not intensively affect the operation of the system when included in the control system, especially with low-tolerance components. Therefore, capacitors with low

discrepancies, below 5%, are suggested for the design, as such values assure the operation of the converter with performance close to the ideal, optimal case.

Moreover, since there are notable momentary current values flowing through the auxiliary capacitances and at high frequencies, components with low ESR and ESL are required, e.g., C0G-based capacitors, so that the dissipated power losses and switching oscillations can be minimized. Nevertheless, when proper capacitors are chosen, their total power dissipation is on a low, negligible level when compared to other power losses in the converter. Thus, auxiliary capacitors in small 2220 SMD packaging with minimal impact on total volume can be employed. Finally, the voltage ratings of the auxiliary capacitors should be capable of sustaining half of the V_{H} voltage plus a margin for voltage overshoots.

Furthermore, it is worth noting that the placement of additional capacitors connected in parallel to each transistor also helps to reduce transistor turn-OFF overvoltages, leading to lower stresses for the power devices.

Besides the crucial auxiliary capacitance optimization, the design procedure has several additional concerns. The system is fully soft-switched but with an increased conduction loss than a more conventional approach. Thus, the choice of power semiconductor devices should focus on minimizing $R_{\mathrm{DS(on)}}$. Moreover, in the proper operation of the converter, the antiparallel diodes do not conduct, so power devices with no additional diodes are recommended in terms of cost. Furthermore, the operating frequency should be maximized. The switching loss is nearly completely eliminated so that inductor size and the volume of other passive components can be minimized, leading to higher power density, with the only constraint of the control system operating speed.

Moreover, as the converter employs fast-switching SiC power transistors, the minimization of parasitics is essential, e.g., shortening the commutation loops. However, as previously mentioned, applying auxiliary capacitances in parallel to the transistor also addresses *dv/dt*-related issues. Thus, the adverse effects caused by stray inductances are minimized, and the design of the converter can be less strict in that regard while the system maintains good switching and EMI performance.

B. Power Losses Calculation

In order to fully determine the benefits of full soft-switching operation using the QSW method, a power loss analysis was conducted. The more thorough operation principle analysis than in [21] also leads to a more precise estimation of the power losses, including the impact of the resonant operation in the currents during the transition states. At first, the always-apparent transistor conduction losses are described by

$$P_{C(Tx)} = R_{DS(on)} I^2_{RMS(Tx)}. \tag{27}$$

However, it is worth noting that, to sustain ZVS at turn ON, the higher the auxiliary capacitance, the higher the current, leading to enlarged conduction losses compared to the conventional TCM-Q2L approach.

Next is the transistor switching loss that can be described by the following equation:

$$P_{SW\_OFF(Tx)} = k_C \frac{V_{DS\_\max(Tx)} i_L(t_5)}{V_d I_d} E_{OFF} f_S \tag{28}$$

where E_{OFF} is the switching-OFF power loss from the datasheet, V_d *and* I_d are the reference voltage and current values. Here, it is assumed that the switching losses are reduced proportionally to the capacitance ratio, described as the output capacitance value divided by the sum capacitance in parallel to the transistor

$$k_C = \frac{C_{oss}}{C_{oss} + C_{aux}}. \tag{29}$$

Thus, when there is no additional C_{aux} capacitance, the capacitance ratio equals 1, and the switching losses are not reduced. Certainly, such a capacitance ratio is a simplification. However, precise calculation of the switching loss reduction is very complex and requires the knowledge of transistor capacitances in the function of voltage, along with a detailed insight into specific transistor turn-OFF times depending on the current, which are rarely provided in the datasheet, that also is used for switching power loss calculation. Therefore, such a simplified approach is sufficient for practical applications, where the main goal is to achieve the highest possible efficiency by finding the optimum between the minimized switching power losses and enlarged conduction and inductor power losses.

The inductor power loss is also essential in addition to the power device loss. The power losses in the core were estimated using the Steinmetz equation, based on the core material (3C92 ferrite) parameters and the magnetic flux calculated employing the inductor current and operating frequencies

$$P_{CORE} = 0.00386 f_S^{\alpha} \frac{L \cdot \Delta i_L}{A \cdot N}^{\beta} \tag{30}$$

where f_{S} is the switching frequency, α and β are constants taken from the core datasheet, L is the choke inductance, A is the core cross section, N is the number of turns, and Δi_{L} is the inductor current ripple.

The total power loss of the inductor, including wire conduction loss, is

$$P_L = R_{WIRE} I^2_{RMS(L)} + P_{CORE}. \tag{31}$$

Finally, the total efficiency of the converter, omitting other, less crucial power loss sources, can be calculated using the following expression:

$$\eta = \frac{P_{OUT}}{P_{OUT} + P_L + P_C + P_{SW\_OFF}} \cdot 100\% \tag{32}$$

where P_{C} is the summarized conduction power loss of all four transistors, and $P_{\mathrm{SW\cdot OFF}}$ is the summarized turn-OFF switching loss of all transistors.

Fig. 3 showcases the exemplary power loss distribution between the cases with (6 nF) and without auxiliary capacitance at 1200 V, $G_{\mathrm{V}} = 0.5$, and 15 kW power. Even though the turn-OFF switching loss is smaller than the already-eliminated turn-ON power loss, it is still apparent due to high switching frequency and high turn-OFF current, and thus notable among total power losses for the system without the auxiliary capacitances. As can

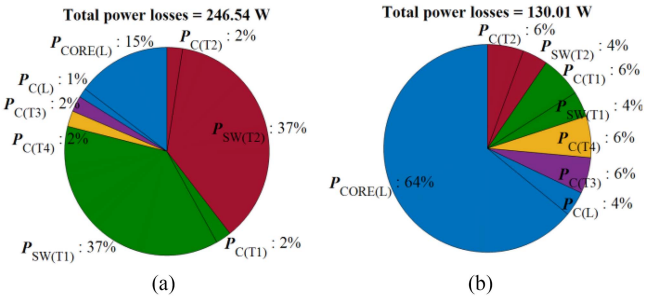

Fig. 3. Comparison of power loss distribution with and without auxiliary capacitance at 1200 V, $G_V = 0.5$, and 15 kW power. (a) $C_{aux} = 0$, (b) $C_{aux} = 6$ nF.

TABLE III
PARAMETERS OF THE CONVERTER PROTOTYPE

Parameter	Description
High-side voltage	800–1200 V
Switching frequency	40–260 kHz
Voltage gain	0–1
SiC power transistors	1.2 kV and 11 mΩ FF11MR12W1M1_B11
Inductor	30 µH/100 A peak
Flying capacitor	330 nF/1000 V
Output/input capacitors	6 µF/1600 V
Auxiliary capacitors	470 pF–10 nF, C0G dielectric

be seen, the loss allocation changes significantly when full soft switching is applied. The transistor losses are lowered to roughly 12 W from over 97 W per device, a substantial value. However, conduction and inductor losses rise due to enlarged currents flowing in the system. The total choke loss rises from around 40 to 88 W, mainly the core losses. However, the total power loss is intensively lowered: from 247 W to just 130 W. Therefore, the use of the method is highly beneficial efficiencywise. Furthermore, as the semiconductor loss is much lower, the heatsink volume can also be vastly minimized. Moreover, it is worth noting that a QSW-controlled system highlights the importance of employing highly performant power electronic chokes.

C. Experimental Results

The experimental study presented in this article is based on the 1.5-kV-rated prototype with C0G SMD small capacitors employed as the auxiliary capacitors, as such dielectric material provides low power loss and high dissipation capabilities. The system parameters are shown in Table III, and the prototype photo is shown in Fig. 4. The converter was tested with a resistive load and supplied by a dc source from Magna-Power (2 × 800 V). The efficiency was measured using the Yokogawa WT5000 power analyzer.

At first, a number of experimental tests were performed for various auxiliary capacitance values to plot efficiency and control characteristics and experimentally validate the optimal C_{aux} value (see Fig. 5), starting from the case with no auxiliary capacitance, up to 10 nF, and also to compare the proposed system with the conventional TCM-Q2L method with no additional capacitance. The tests were performed at 800 V dc input voltage

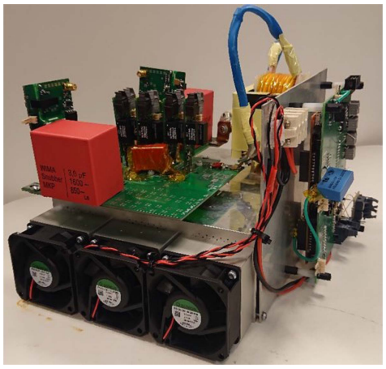

Fig. 4. Photo of the constructed converter prototype.

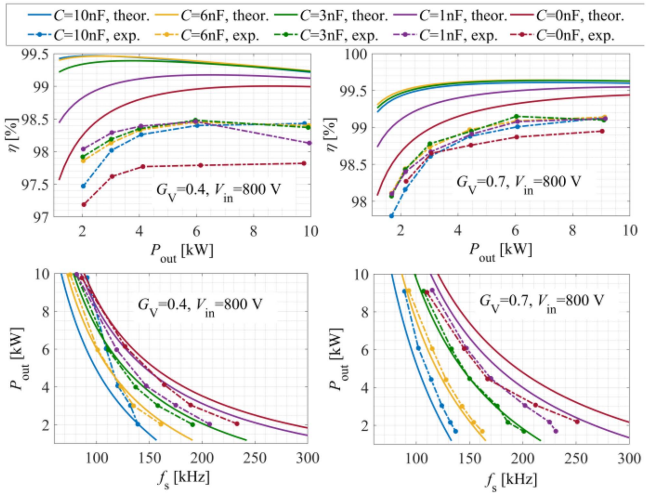

Fig. 5. Efficiency and control characteristics for various C_{aux} values: with 0.4 voltage gain (left) and with 0.7 voltage gain (right) performed at 800 V dc.

V_H and up to 10 kW power. All the experimental results are also supported by its theoretical outcomes, both for efficiency and control characteristics. However, as usual, a difference between the theoretical and experimental efficiencies can be seen, most likely due to a nonideal description of the inductor loss, omitted capacitor, and path resistance losses, and additional soft-switching residual loss [28], [29], which even if very small one-by-one, for such a high efficiency are still visible in total. Furthermore, the discrepancies between the experimental and theoretical results are especially visible for low power, most likely due to lowered frequency because of calculation errors in the converter control system, leading to higher rms currents.

As mentioned before, the value of auxiliary capacitance has a notable effect on the control characteristic: the higher the capacitance, the higher the rms transistors and inductor current, and the lower the switching frequency. Moreover, a change in efficiency can be observed as well. The C_{aux} values below 3 nF do not ensure satisfying turn-off switching loss reduction, while those above 6 nF provide too many additional power losses via enlarged inductor current and the following power losses.

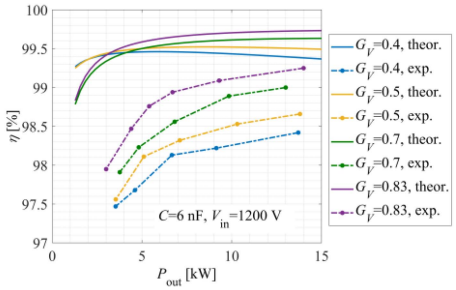

Fig. 6. Efficiency characteristics for optimal C_{aux} value of 6 nF and up to 15 kW power with various values of constant voltage gain.

All in all, based on the abovementioned experimental results, and including the theoretical efficiency analysis for auxiliary capacitor optimal value selection described before, 6 nF C_{aux} was chosen as the optimal value for high power operation. This is because of two main factors: one is the high efficiency, and the other is limited output voltage ripples due to still high operating frequency.

Furthermore, experimental tests up to 15 kW at 1200 V high-side voltage V_{H} were performed using this capacitance (6 nF) so that additional characteristics for different loads and voltage gains (see Fig. 6) could have been plotted. As can be seen, significant efficiencies are achieved, especially for higher power, lighter loads, and voltage gains higher than 0.4, confirming the remarkable capabilities of the proposed system. Simultaneously, at low output power, the highest efficiency was achieved for auxiliary capacitance $C_{\mathrm{aux}} = 1$ nF (see Fig. 5). This is due to the low value of transistor turn-OFF current and high switching frequency; at high frequency, the resonant operation occurs for the major part of the switching period with increased conduction losses. That effect is also increased by increasing C_{aux}, leading to an enlarged resonant period.

Fig. 7 presents exemplary experimental results with peak recorded efficiency of 99.5%, showcasing the waveforms expected in a properly operated system, with full soft-switching assured due to added C_{aux} and appropriate control. This test was performed with optimal 6-nF auxiliary capacitance, 800-V V_{H} dc voltage, nearly 10 kW power, voltage gain of roughly 0.91, and 40-kHz switching frequency. As can be observed, the soft-switching process is apparent for both turn ON and turn OFF, which is confirmed by comparing the $v_{\mathrm{GST1(th)}}$ voltage with the transistor threshold voltage, as well as through constant dv/dt slopes in both v_{DS} and v_{IND} voltages. As can be seen, the transistor is turned OFF close to 0 V when the voltage has just started to rise and is turned ON when the voltage is already below 10% of the OFF-state voltage (roughly 35 V compared to 400 V in off-state), which in conjunction with the fact that at this moment the drain current just slowly starts to rise, limits the switching losses to negligible values, and the efficiency can rise to high levels (peak at 99.5%), especially for higher power, as for such conditions, the converter operates with low switching frequency, which minimizes the choke core power losses, which are the main source of losses in the system (see Fig. 3).

Finally, an experimental comparison for dv_{DST1}/dt rising slopes and transistor turn-OFF switching process for various C_{aux}

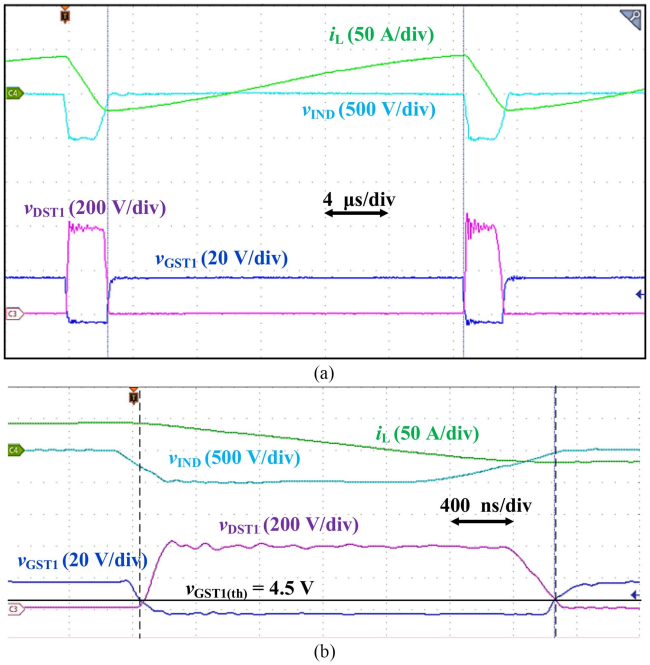

Fig. 7. Experimental results for the test with peak recorded efficiency of 99.5%, performed at $V_{\mathrm{H}} = 800$ V dc voltage, nearly 10 kW power, frequency of 40 kHz, and G_{V} of 0.91: (a) general view, (b) zoomed view.

values is exhibited in Fig. 8. As can be seen, the capacitance value greatly affects the voltage rising slopes as the rise time changes from 47 ns and no auxiliary capacitance, up to roughly 197 ns at 10 nF C_{aux} value. More specifically, the dv_{DST1}/dt varies from 8.51 V/ns for no C_{aux} up to 2.03 V/ns for the case with $C_{\mathrm{aux}} = 10$ nF, which directly affects at what v_{DST1} voltage the transistor switches and, in consequence, what is the turn-OFF power loss. Increasing C_{aux} leads to a lower dv_{DST1}/dt ratio, e.g., as shown for the case with $C_{\mathrm{aux}} = 10$ nF, where the transistor is turned OFF at nearly 0 V v_{DST1} voltage, which results in negligible turn-OFF power losses. Simultaneously, according to the mathematical analysis presented in Section II, increasing the auxiliary capacitance leads to a longer resonance process and higher resonant currents, which negatively impacts the converter's efficiency—despite lowering turn-OFF power losses, other losses, e.g., conduction losses are enlarged. Therefore, optimal selection of C_{aux} value is necessary for maximizing the efficiency.

Moreover, aside from helping to intensively reduce the turn-OFF power loss according to the analysis shown in the article, the increased rising times also positively affect the possible EMI-related issues that would be caused by the rapid switching times of conventionally switched SiC MOSFETs.

IV. Performance Comparison

The comparison of the proposed fully soft-switched TCM-Q2L converter with several state-of-the-art converters is shown in Table IV. When comparing with the foremost competitors, the conventional TCM-Q2L [21] and TCM-3L [18] converters, with only partial soft-switching, it can be observed that an

TABLE IV
COMPARISON OF THE PROPOSED CONVERTER WITH OTHER THREE-LEVEL-BASED STATE-OF-THE-ART SYSTEMS

Parameter	Hybrid resonant converter [9]	ZVT converter [16]	TCM-3L converter [18, 23]	TCM-Q2L converter [21]	Proposed converter
MOSFET no.	4+4	4+2	4	4	4
V_{DS_max}	V_H at boost stage (4) $V_H/2$ at resonant stage (4)	$V_H/2$	$V_H/2$	$V_H/2$	$V_H/2$
Conduction mode	near-CRM	CCM	near-CRM	near-CRM	near-CRM
Soft switching	**Full at resonant stage, none at boost**	**Full**	**Full at turn on, partial at turn off**	**Full at turn on, partial at turn off**	**Full**
Additional components	Additional *LC* circuit in resonant stage	Two ZVT cells, each comprised of a transistor, a capacitor and two inductors	RC snubbers recommended	RC snubbers recommended	Four auxiliary capacitors in parallel to each transistor
Flying capacitance	-	-	High	Very low	Very low
Choke inductance	Medium	Medium	Very small	Small	Small
RMS choke current	High	Low	High	High	High
Efficiency	**Extremely high**	**High**	**Very high**	**Very high**	**Extremely high**

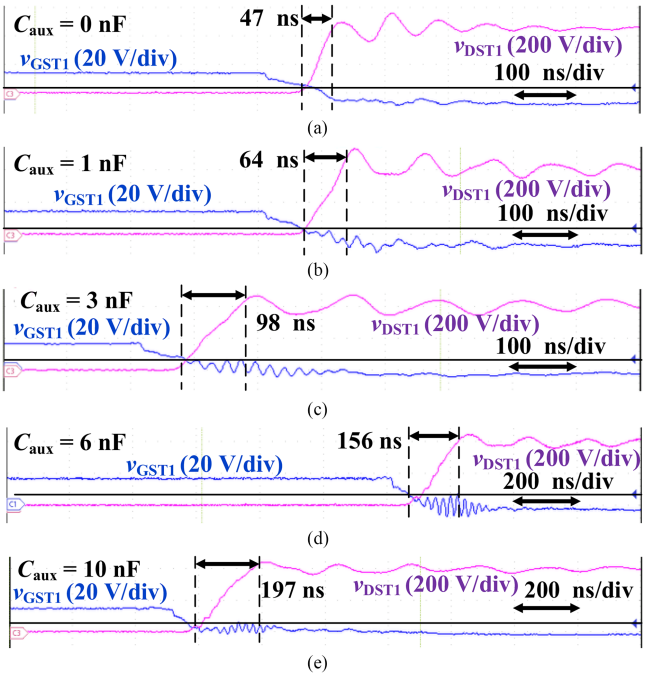

Fig. 8. Experimental comparison for dv_{DST1}/dt ratios and turn-OFF switching process for different C_{aux} values with highlighted $v_{GS(th)}$ threshold voltage (4.5 V). Tests performed at roughly 10 kW power, 800 V V_H voltage, G_V of 0.7, and peak inductor current at approximately 43 A. (a) $C_{aux} = 0$ nF. (b) $C_{aux} = 1$ nF. (c) $C_{aux} = 3$ nF. (d) $C_{aux} = 6$ nF. (e) $C_{aux} = 10$ nF.

improvement in efficiency is visible due to full soft-switching, also at turn OFF, where the conventional approach has two transistors hard-switching at turn OFF. On the other hand, higher sum output capacitance leads to lower operating frequencies, negatively impacting the voltage ripples. Still, this may be easily circumvented using lower choke inductance, which can in total also positively affect total volume. All in all, when the current ripple is concerned, in the designing process for both conventional and fully soft-switched TCM-operated systems, the desired frequency should be assumed, leading to specific current ripples for the application and the difference in choke inductances being visible for both cases. Furthermore, to achieve the mentioned ZVS at turn OFF, auxiliary capacitors are required in parallel to each transistor. However, using C0G dielectric-based capacitors, the volume increase is negligible, and the additional cost is also insignificant compared to the cost of the rest of the converter. Additionally, in the conventional approach to the TCM operation, it is often recommended to add RC snubbers to suppress the overvoltages nevertheless. All in all, the proposed converter seems to be the superior choice, and the small extra effort required for employing the full soft-switching through additional auxiliary capacitances is well justified for efficiency-oriented applications.

Moreover, the proposed system can be further deemed highly competitive also concerning other dc/dc converters: when compared with the hybrid resonant converter shown in [9], similarly high efficiency is achieved, but with a much lower number of power semiconductor devices; while compared to the ZVT converter [13] the achieved efficiencies seem higher, and also with a lower component count. Finally, it is worth noting that the proposed method for achieving full soft-switching can be further adopted into conventional TCM converters, both in dc/dc and inverter applications, in two level and multilevel configurations.

V. CONCLUSION

An investigation into the effects of QSW-based soft-switching applied to a Q2L-controlled nonisolated dc/dc flying capacitor converter was presented in this article. It was shown that the system based on a conventional flying capacitor converter leg using TCM-Q2L control, with the novelty in the form of small auxiliary capacitors added in parallel to the MOSFETs assuring full soft-switching throughout a wide operating range, can be designed and constructed using the QSW method. Such a system was characterized by ultra-low power loss and reduced *dv/dt* ratio, which allows for full utilization of the SiC power devices at high frequencies and voltages, with low regard to the switching loops of the converter. Moreover, the presented system, when compared with conventional TCM-based approaches, showed even higher efficiency and, considering the possible reduction of inductance because of the lower operating frequency, can be considered beneficial also volumewise. The key contribution

of this article was showcasing the impact of additional C_{aux} capacitors in the TCM-controlled system, which provided full soft-switching contrary to conventional TCM-based converters, as well as optimal capacitance value selection for maximizing efficiency. The study was supported by experimental tests validating the noteworthy merits of the high-frequency converter up to 15 kW, with the peak efficiency reaching as high as 99.5%, which was a significant value compared to other state-of-the-art dc/dc solutions in the MV range.

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Chapter 4

Conclusion

The thesis contains an investigation of medium voltage SiC-based power converters on the basis of five publications [P1-P5]. The considered topics include the modeling and characterization of SiC MOSFETs, mainly considering high-power power modules. Furthermore, the subject of loss estimation is studied, and experimental emulation of a SiC MOSFET power module operating in an MV power converter is exhibited. The presented could be beneficially employed to improve the designing process of high-power MV converters. Moreover, several different techniques for designing MV systems are presented and compared based on an experimental evaluation, ranging from single-device two-level topologies through series-connection of transistors, conventional multilevel approaches, e.g., FC converter, as well as the emerging quasi-two-level technique. The detailed overview could be used as a guideline for designers seeking a fitting topology for specific MV converters. Finally, the thesis encloses a novel, highly efficient, and compact dc-dc non-isolated converter with soft-switching as an example of a system that allows for the appropriate utilization of SiC power devices, presenting several notable advantages over conventional Si-based systems. Thus, the proposed techniques can be effectively employed to improve future MV power converters.

The issues regarding the modeling and characterization are studied in [P1]. Using the proposed novel concept, the SiC MOSFET power module output capacitances can be characterized easily, which is a necessity in order to establish power losses of the power devices properly. The method is also especially important in the designing process of high-power MV converters, for when a power of hundreds of kilowatts is taken into account, even an error below 1% equals to a substantial power loss mismatch, which could lead to an inefficient design, both in terms of loss and thermal operation.

The exhibited method is very simple and requires a straightforward setup akin to single- or double-pulse test benches. Thus, the realization and cost effort is minimal. Moreover,

the importance of the proposed method is further accentuated, as for many SiC power modules under development, the capacitance characteristics are not readily available. Thus, the novel technique could be an invaluable tool for designing highly efficient and compact power converters in the medium voltage range.

The topic of power loss estimation is further investigated in [P2]. The paper introduces a new method for power loss emulation that could be employed in the designing process of MV high-power converters so that an accurate estimation is achieved, which is essential for the proper design of the system. The proposed approach is especially valuable because the parasitics are of great importance for the SiC-based systems. Thus, since the values from the datasheet are established for a specific circuit, with particular parasitics, they cannot be easily applied for the design of the converters, and other methods to establish the power losses need to be introduced, e.g., as proposed in the paper.

Furthermore, the proposed approach is a simple and cost-effective solution. The required setup is very similar to a conventional double-pulse setup and only requires supplying the power losses of the SiC-based power modules. Thus, a several hundred-kilowatt system can be emulated using just a few kilowatts from the source. In the end, the suggested method could significantly enhance the design of prominent MV power converters of the future.

While there have been many approaches to constructing MV power converters proposed in the literature, these were mostly studied separately. Therefore, in [P3], a comprehensive experiment-based comparison is showcased, establishing the traits of each method. The considered solutions include two-level topologies with single devices with notable blocking voltages, the series connection of LV transistors employing active voltage balancing, conventional multilevel topologies on an example of an FC structure, and the emerging Q2L technique seen as a convergence of the two latter.

The discussed methods are compared using a multi-criterion approach. The foundation of the study are the physical models of each option, tested at up to 1.5 kV and 300 A rms. Based on the prototypes, crucial practical characteristics are established, i.e., the power loss is defined, and the design considerations and complexities are taken into account, including gate drivers, cooling measures, and power circuit layout, as well as the control of the systems. Furthermore, the reliability and cost are also evaluated. In the end, the provided detailed observations could be effectively used as a reference for MV power electronics designers seeking the most appropriate topology for their specific applications.

As an illustration of the possibilities of SiC-enabled MV power electronics, novel dc-dc converters are proposed in [P4] and [P5]. The systems are based on a new TCM-Q2L method, converging the prominent Q2L method to effectively employ LV devices, akin to

series connection but with a straightforward lossless voltage balancing and TCM approach that enables soft-switching at turn-on, minimizing the switching losses, allowing for reaching high frequencies which lead to higher power density.

The general concept, with a thorough mathematical analysis, is presented in [P4]. Moreover, a simple voltage balancing control loop is proposed, assuring safe operating voltages for the SiC switches. The proposed converter is further enhanced in [P5] by adding supplementary, minuscule capacitors in parallel to each transistor, allowing even higher efficiencies, as the soft-switching at turn-off is also ensured. A detailed investigation into the capacitor-enabled QSW is also exhibited, providing comprehensive design guidelines for maximizing efficiency. Apart from lowering the power losses, the proposed technique also minimizes the transistor dv/dt ratio, which helps to negate the adverse effects of parasitics and fully utilize SiC power devices in MV applications.

Overall, the proposed MV dc-dc converter is characterized by an outstanding performance in terms of low-loss operation and power density, reaching efficiency as high as 99.5%. The system has been validated at up to 1.5 kV, 15 kW of power, and a switching frequency of up to 250 kHz, depending on the operating point. The novel approach is proven to be a highly competitive choice for MV dc-dc power conversion, clearly surpassing conventional Si-based solutions and reaching as good if not better performance compared to other state-of-the-art MV converters employing SiC MOSFETs, deeming it a perfect choice for future power electronics applications such as traction, e-mobility, PV, and battery energy storage systems.

The aim to study the possibilities of effective electric energy using SiC-based medium voltage power electronics, and the other specific goals have been reached. As shown in the dissertation, the converter design process can be improved by employing the proposed methods for transistor characterization and power loss estimation. Furthermore, the performed experimental-based comparison showcases the vast array of possible converter topologies applicable in medium voltage, and can be used as a guideline for choosing an appropriate approach for a specific power electronics application. Finally, it is shown that by employing the proposed novel techniques for an MV dc-dc converter, a highly efficient power converter, operated at a notable frequency, can be constructed and effectively and competitively employed in MV power electronics applications.

The area for future works is quite broad, as the subjects considered within the dissertation are vast. When the modeling of SiC MOSFETs is considered, there are still several issues regarding the proper description of the switching process, especially in the case of the turn-off procedure, as prior works have not included all critical traits of Silicon Carbide, e.g., the

threshold voltage shift. Furthermore, an extension for other, more sophisticated converter topologies, e.g., multilevel, may be given for the proposed power loss emulation method. When the methods for designing MV systems are taken into account, the analysis could be expanded into high voltage range or for specific applications. Considering the proposed novel concepts for dc-dc converters, these could be applied to other types of converters, e.g., inverters, or a system for a higher voltage employing multiple transistors in a stack could be studied. Overall, as medium voltage power electronics are becoming more common, the topic should remain of a great interest for researchers and engineers alike.

The contribution of the dissertation author can be summarized as follows:

- a review of methods for the construction of power converters for medium voltage systems, including the possible applications,
- a brief overview of Silicon Carbide power devices,
- proposing novel concepts for medium voltage power converters, e.g., the TCM-Q2L and QSW methods,
- performing advanced simulation study regarding medium voltage power electronics,
- design & construction of experimental setups and converters rated at medium voltage,
- performing experimental study on medium voltage prototypes,
- preparing publications in top journals (summarized Impact Factor for the core papers – 26.189, total points according to the Ministry of Education and Science – 740),
- presenting the results at several international conferences.

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